VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

SHARP TECHNICAL MANUAL

T09P3VC-A615X

VHS VIDEO CASSETTE RECORDER

(PAL SYSTEM)

SERIES	MODEL NO.	VIDEO HEAD
VC-A103 Series	VC-A103R(BK), Q(BK), GV(BK), VC-A106GVM(BK)	2-head system
VC-A116 Series	VC-A116S(BK), B, K, E, W, VC-B322N	
VC-A125 Series	VC-A125X	
VC-A215 Series	VC-A215S(BK)	
VC-A118 Series	VC-A118D	
VC-A508 Series	VC-A508DT	Double azimuth 4-head system
VC-A615 Series	VC-A615G(BK), S(BK), GM(BK), SM(BK), YM(BK), HM, X, WT, NZ, VC-B377N, NT	
VC-T620 Series	VC-TN623QM(BK)	
VC-A215 Series	VC-A215H	2-head LP system

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SHARP CORPORATION

1. MECHANISM

OUTLINE

This VTR is a low-profile, shelf-mount type working on the VHS system. Many newly developed mechanisms have been adopted to make this model thinner, more reliable and power-saving compared to the conventional models.
Main features include:

1) Use of a single-cam system which can cope with various modes
2) A newly developed thin capstan DD (Direct Drive) motor
3) Appropriate torques achieved by a geared reel drive system
4) Newly developed loading system for systemization of the cassette control and loading mechanisms

CONFIGURATION

The mechanism of this model can be roughly divided into the following sections.
System sections

1) Tape drive train system
2) Loading mechanism
3) Cassette tape take-up mechanism
4) PAD (Power Assist Drive) mechanism
5) Cam switch
6) Cassette control mechanism

These sections are discussed one by one as follows.

1-1. Tape Drive Train System

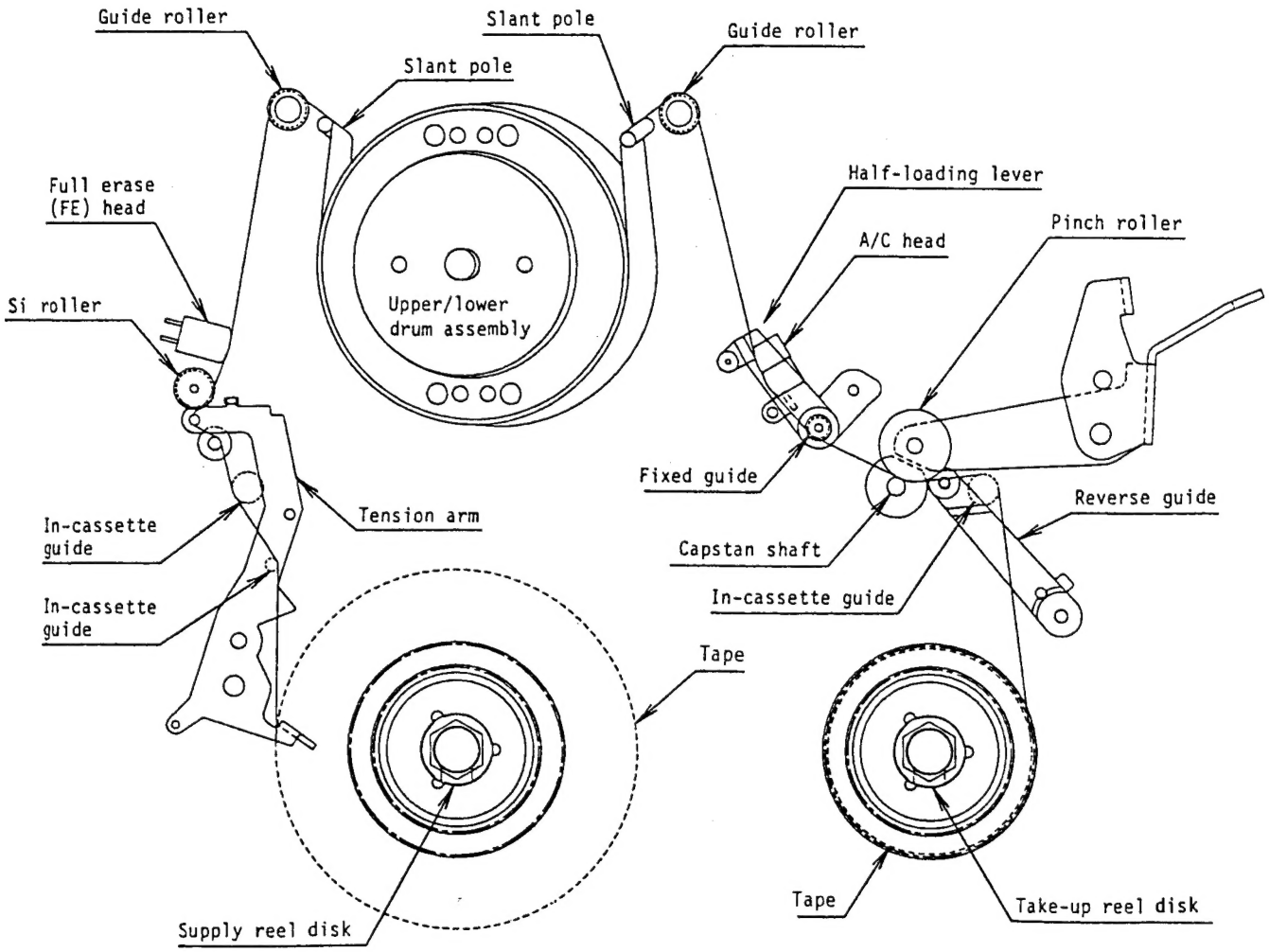


Figure 1-1. Tape Travel System

Features

1) Miniaturized Si (Supply impedance) roller from 16 mm to 7 mm dia.; much smaller mechanism realized.
2) Fixed erasing head; simple design.
3) Enlarged guide roller from 6 mm to 7 mm dia.; reduces the number of revolutions in high-speed video search operation.
4) Miniaturized pinch roller from 18 mm to 14 mm dia.; subcompact mechanism accomplished.
5) The reverse guide works in Video search (VS) and rewind (REW) modes only, reducing the risk of tape damage.

1-2. Loading Mechanism

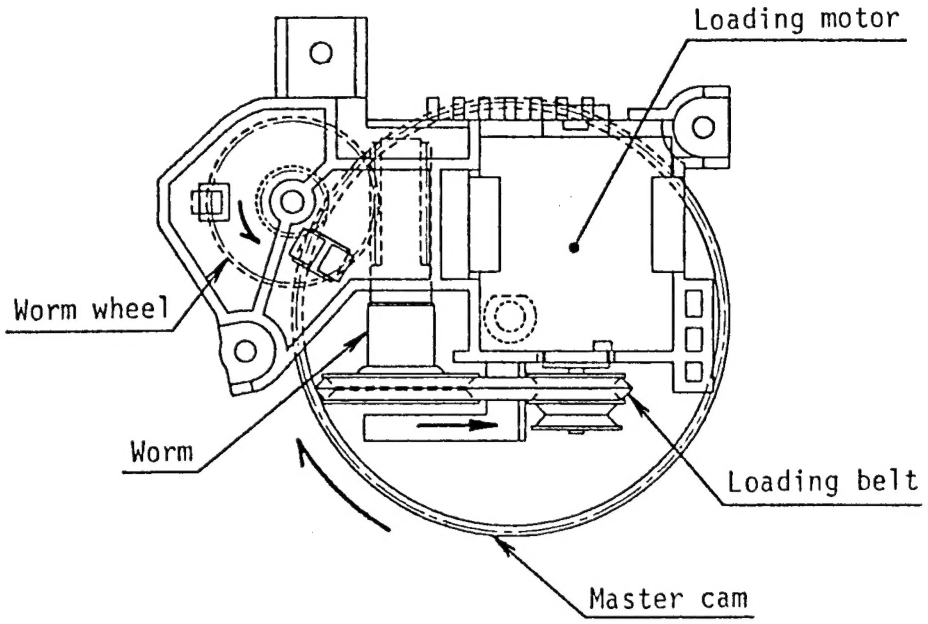


Figure 1-2. Loading Mechamism (Upper stage)

Features

1) The mechanism is driven by the loading motor.
2) The loading motor is intended to drive the mechanism and the cassette housing.
   (Refer to the description on the clutch shifting mechanism on page 17.)
3) The four-cam system which used to control the operation of the whole transport mechanism has been combined into a single master cam.

1-3. Cassette Tape Take-up Mechanism

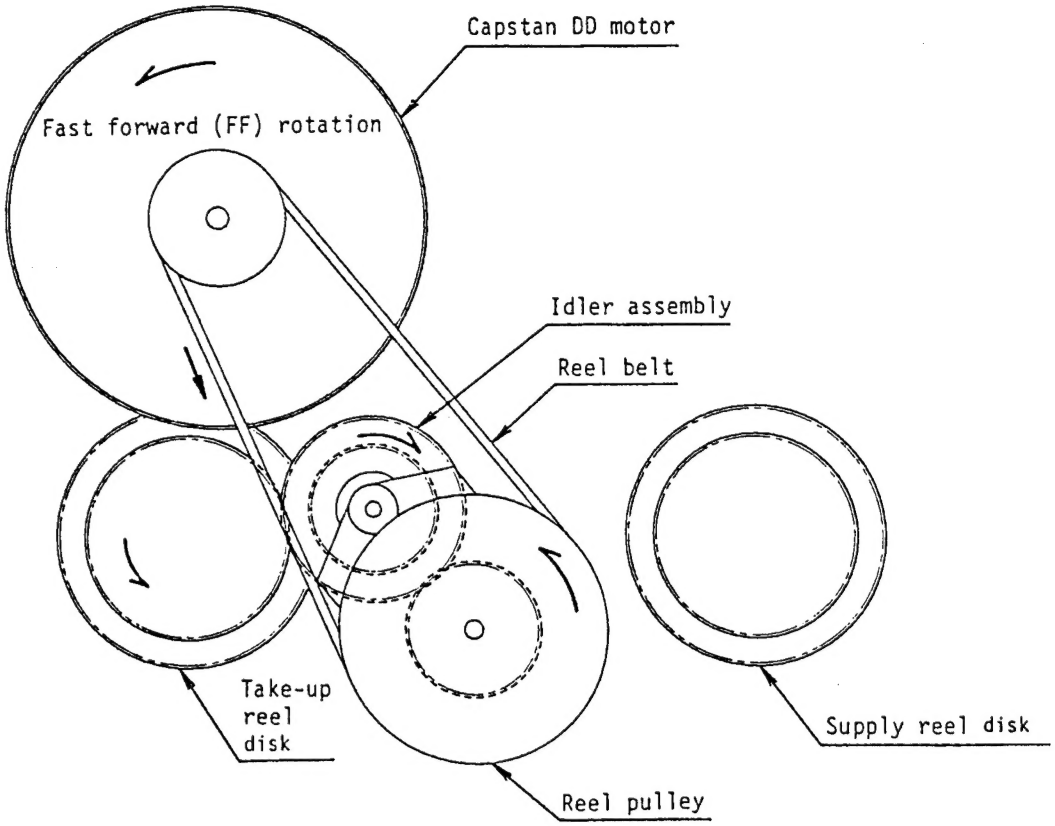


Figure 1-3. Cassette Tape Take-up Mechanism 1 (Lower stage)

Features

1) The reel disk to be driven by the idler assembly is switched by changing the rotational direction of the capstan DD motor.
2) The reel pulley and the idler assembly are always engaged with each other, and the rotation of the capstan DD motor is transmitted through the reel belt to the supply or take-up reel disk.
3) The idler assembly consists of a large and a small gear in a monoblock construction and mounted in the mechanism to allow vertical slide operation.
4) Each reel disk incorporates a slip mechanism to take up the tape without any slack and at an appropriate take-up torque in recording, playback and trick play operations. (large gear)

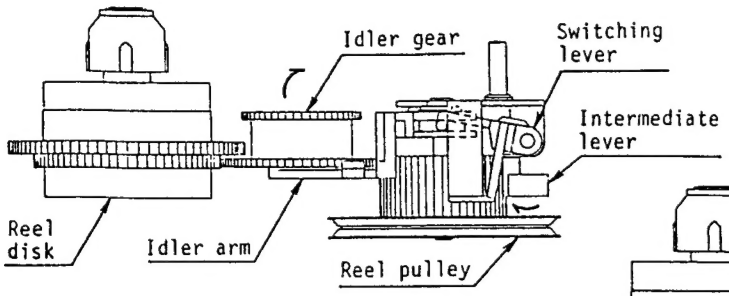


Figure 1-4. Gear Engagement in Fast Foward and Rewind Operations

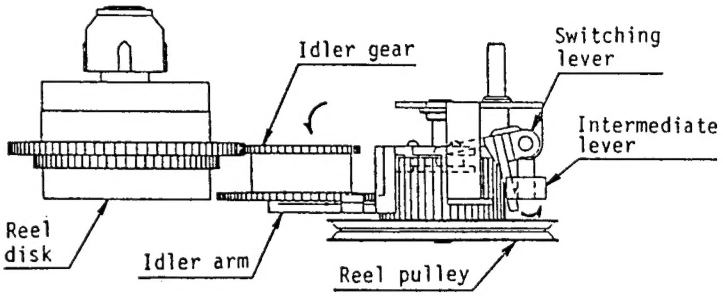


Figure 1-5. Gear Engagement in Recording, Playback and Trick Play Operations

5) In the fast forward and rewind modes, the large idler gear engages with the small gear of the reel disk, not through the torque limiter built in the reel disk. They work as a simple gear mechanism to transfer the revolving motion to the reel disk. (Figure 1-4.)
6) In the recording, playback and trick play modes, the idler arm moves to the lower position so that the small idler gear engages with the large gear of the reel disk. In this case, the rotation of the idler assembly is transmitted through the torque limiter built in the reel disk to the reel disk. (Figure 1-5.)

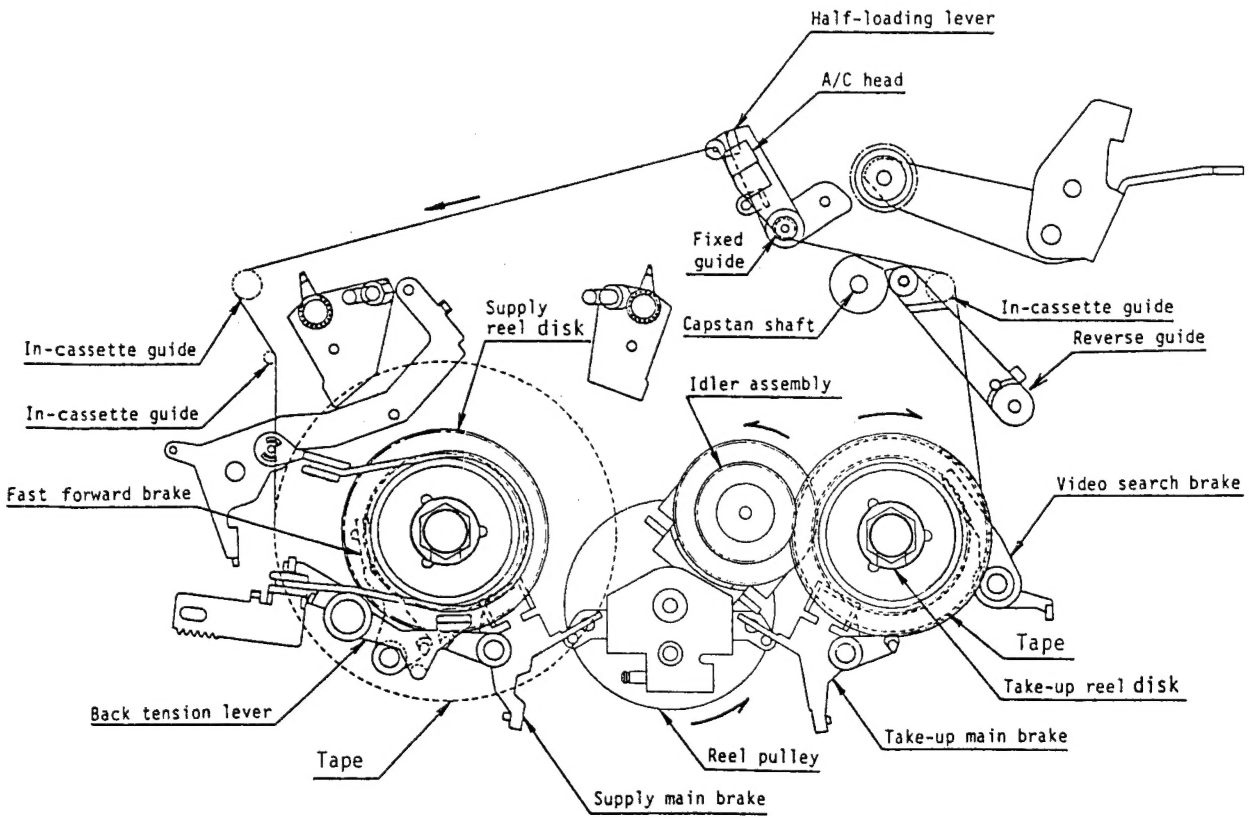


Figure 1-6. Cassette Tape Take-up Mechanism 2 (Upper stage)
Fast forward operation

7) In fast forward and rewind operations, a back tension is provided by the fast forward brake and video search brakes. (Figures 1-6. and 1-7.)
8) The idler gear is positioned as shown in Figure 1-5. when tape loading is completed. The limiter gear of the take-up reel disk then goes into an operating condition, and its sliding motion absorbs the change in tape diameter while the tape is being wound in order to compensate the reel's revolving speed. (Figures 1-5. and 1-8.)
9) In playback and recording operations, a back tension is provided by a combined force of the tension band, tension arm and tension spring at the supply reel disk. (Figure 1-8.)
10) The back tension in the VS and REW modes is given by the video search brake for the take-up reel disk. (Figure 1-9.)

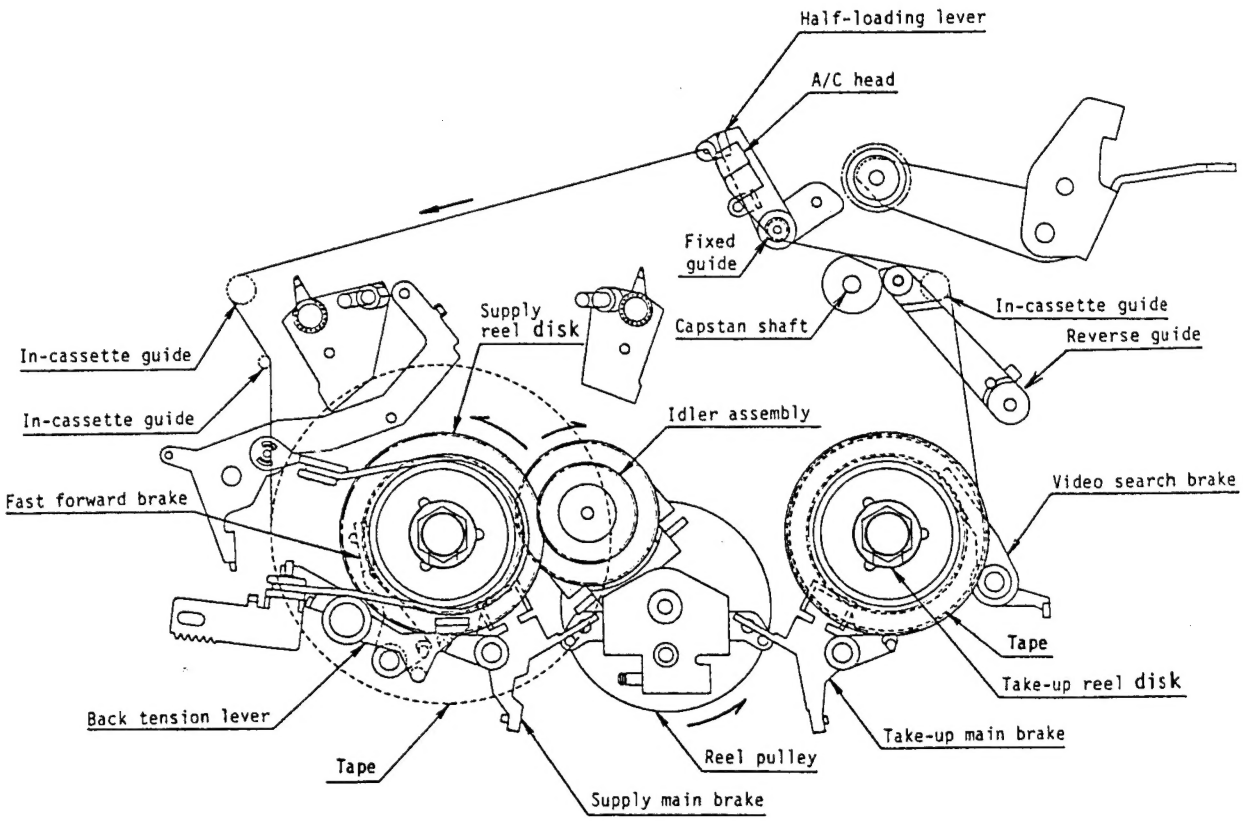


Figure 1-7. Cassette Tape Take-up Mechanism 3 (Upper stage)
Rewind operation

11) In the VS and REW modes, the tension release lever slackens the tension band so that only the brake of the back tension lever acts on the supply reel disk. (Figure 1-9.)
12) The reverse guide works in the VS and REW modes in order to stabilize tape drive train during reverse running. (Figure 1-9.)

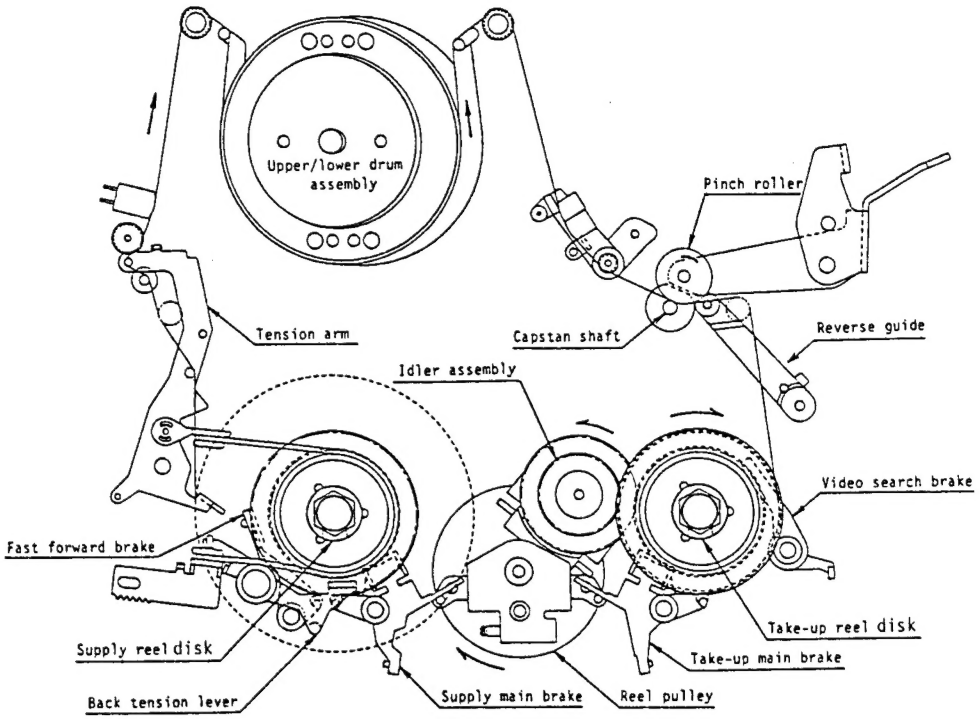


Figure 1-8. Cassette Tape Take-up Mechanism 4 (Upper stage)
Recording and playback opertions

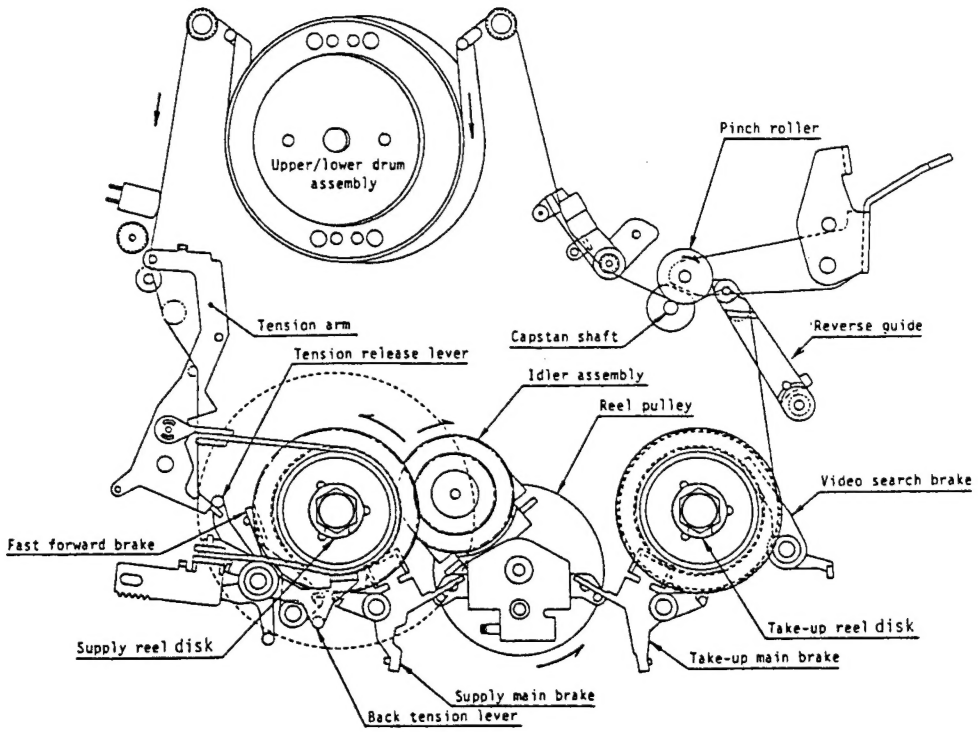
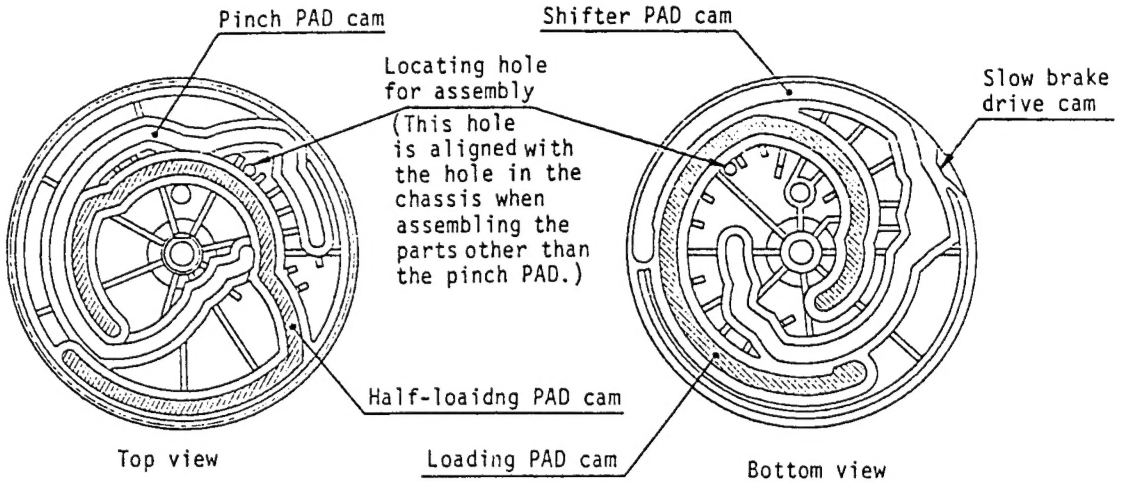


Figure 1-9. Cassette Tape Take-up Mechanism 5 (Upper stage)
VS and REW operations

1-4. PAD (Power Assist Drive) Mechanism

1) Master cam grooves

As shown in Figure 1-10., the single master cam has some grooves on its both sides to bring the mechanism in various modes. The control levers are guided along these grooves. Precise switching is also guaranteed with the interlocking of this cam and the cam switch.



Figue 1-10.

2) Positional relation and operation of loading gears

The loading gear S is aligned with the loading gear T so that the locating mark 1 (round projection) of the former gear engages with the notch on the circumference of the latter gear. See Fig. 1-11.

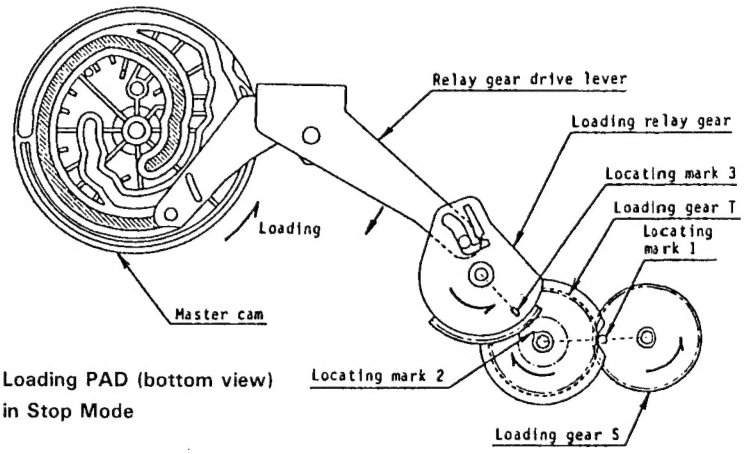


Figure 1-11. Loading PAD (bottom view) in Stop Mode

Next, the locating mark 2 of the small gear of the loading gear T is aligned with the locating mark 3 of the loading relay gear.

Figure 1-11. and Figure 1-12. show the positional relation in Stop and Play mode, respectively. Note the difference in the position of the relay gear drive lever with respect to the master cam groove between two modes.

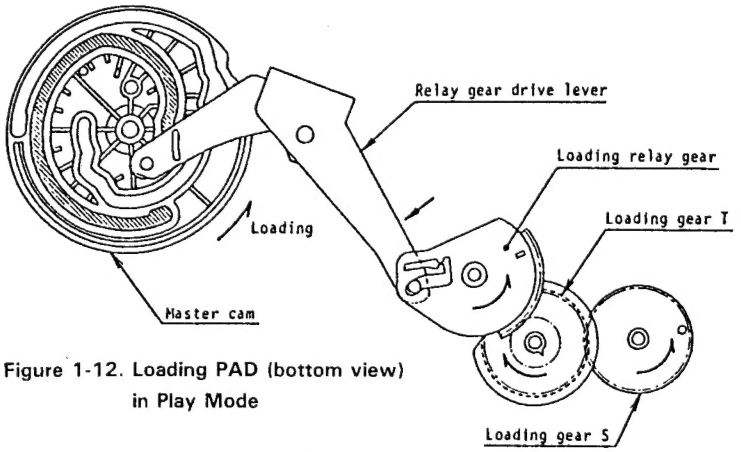


Figure 1-12. Loading PAD (bottom view) in Play Mode

3) Positional relation and operation of pinch roller lever (other than in eject operation)

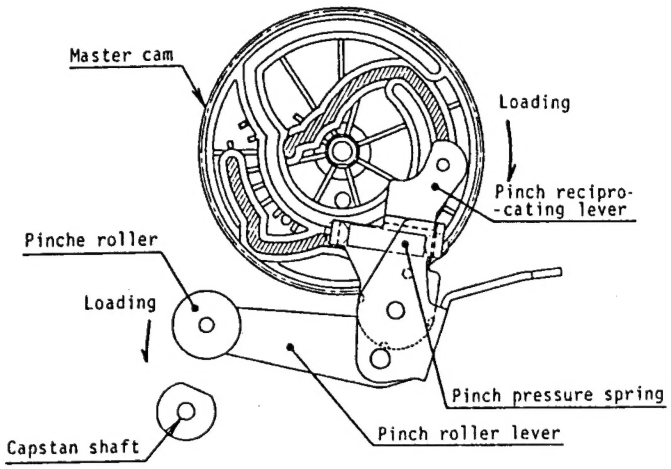


Figure 1-13. Stop Mode (FF/REW)

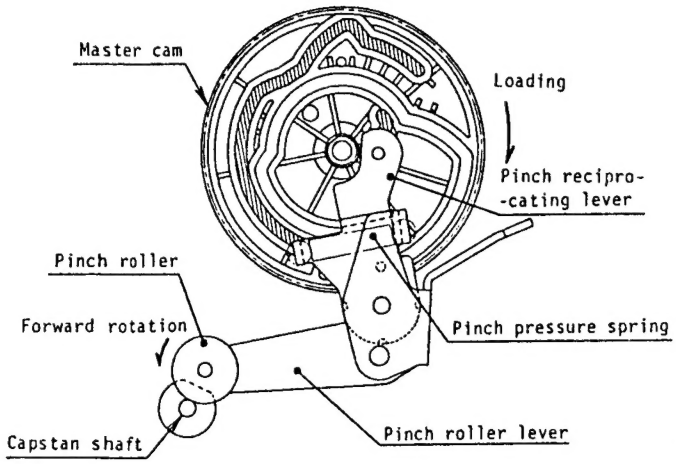


Figure 1-14. Playback Mode

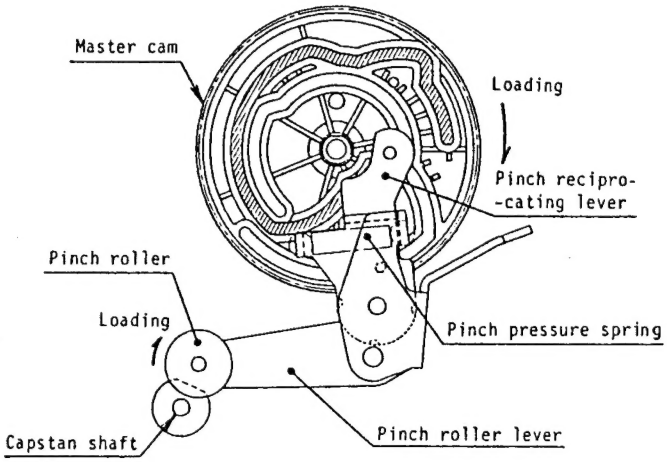


Figure 1-15. Positioning in Pause Mode

When the pinch roller has been pressed against the capstan shaft, the master cam rotates to the position shown in Figure 1-14. Then, the pinch pressure spring gives a necessary pressure (1,000 - 1,200 g) to feed the tape.
Just before going to the video search rewind mode or at short rewind operation in the REC/PAUSE mode, the master cam once rotates to the position shown in Figure 1-15. to slightly release the pinch roller pressure; this is just to allow the capstan to feed the tape while the idler assembly is shifting toward the supply reel disk. Then, it reverts to the position shown in Figure 1-14. and feeds the tape in the reverse direction to ensure stable tape reversing.

4) Operation of half-loading lever

- The cassette is loaded in the normal position only in the FF and REW modes by the master cam and released in the other modes.
- The half-loading lever is always kept at a fixed position by the half-loading reciprocating lever, half-loading reciprocating spring and half-loading drive lever.

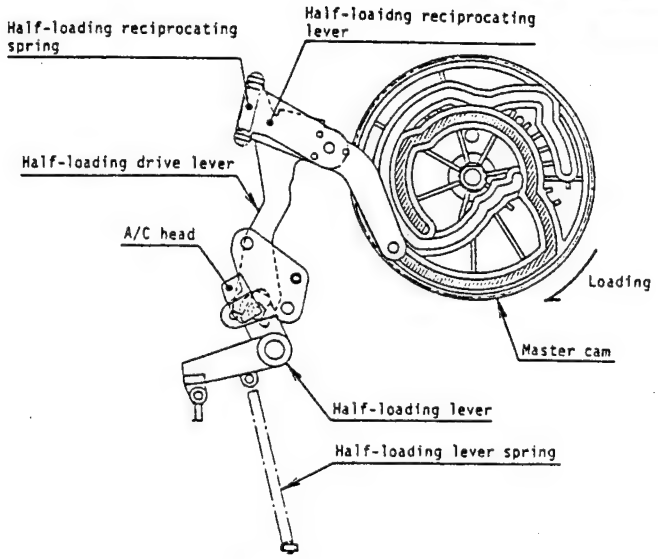


Figure 1-16. Eject Mode

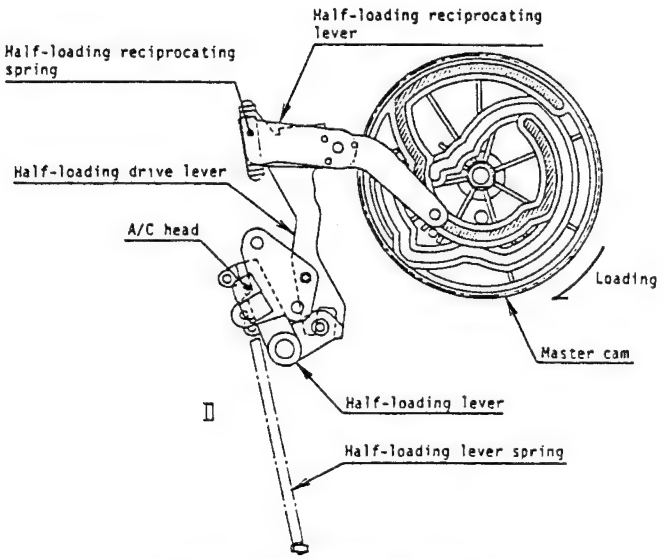


Figure 1-17. Stop Mode (FF/REW)

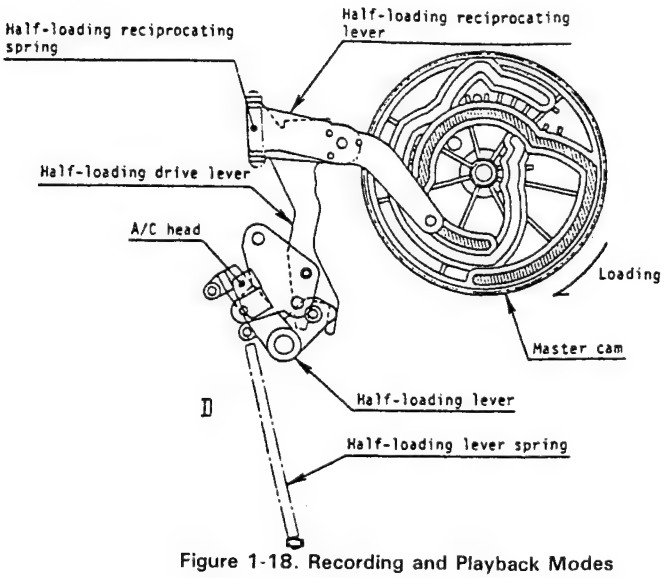


Figure 1-18. Recording and Playback Modes

5) Operation of brake shifter

The relay shifter transfers the driving force of the master cam to the brake shifter to cause a linear motion of the brake shifter as shown in Figure 1-19.

The brake shifter performs the following operations:

- Activation and Releasing of the main brake
- Vertical movement of the idler lever
- Activation and Releasing of the fast forward brake
- Activation and Releasing of the back tension brake
- Switching of the driving force of the video search brake
- Releasing of the tension arm

Further, the relay shifter performs activation and releasing of the reverse guide.

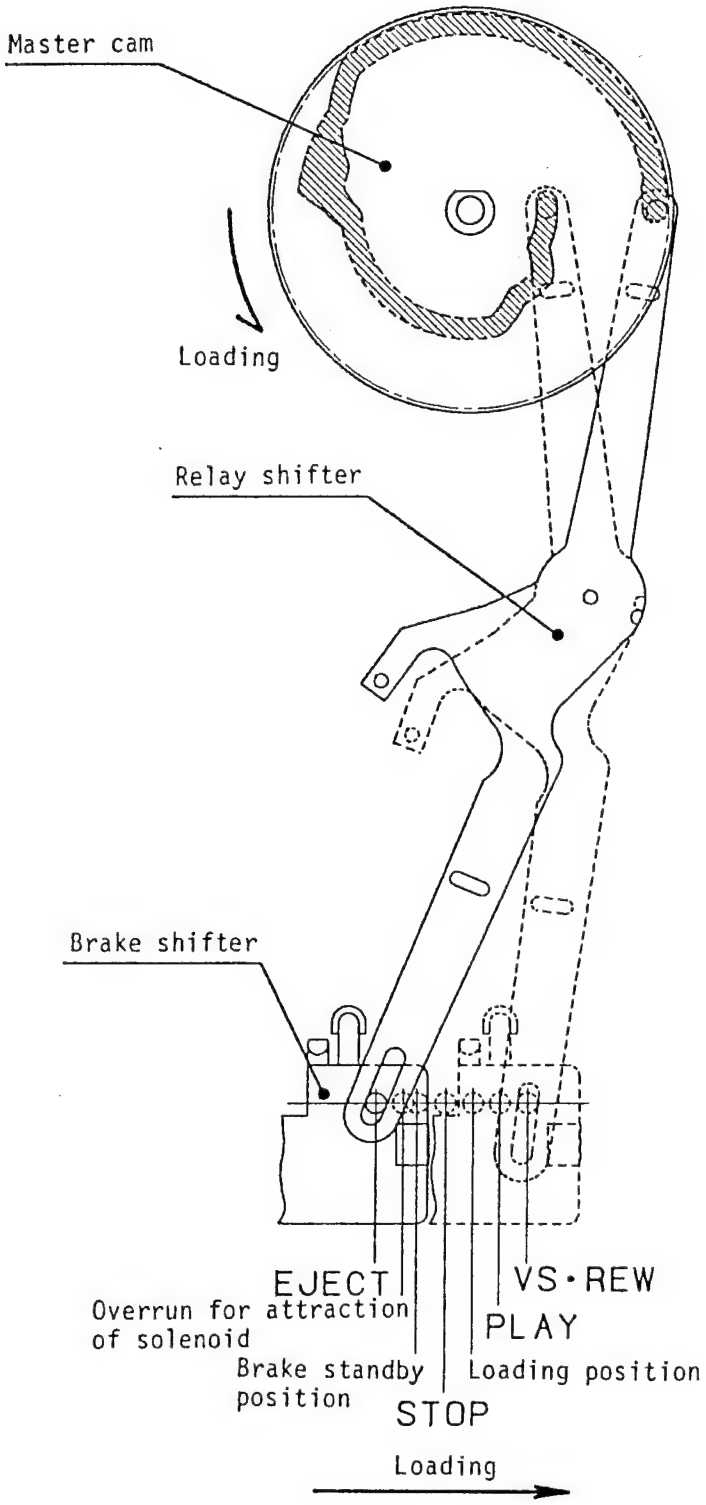


Figure 1-19.

1-5. Cam Switch

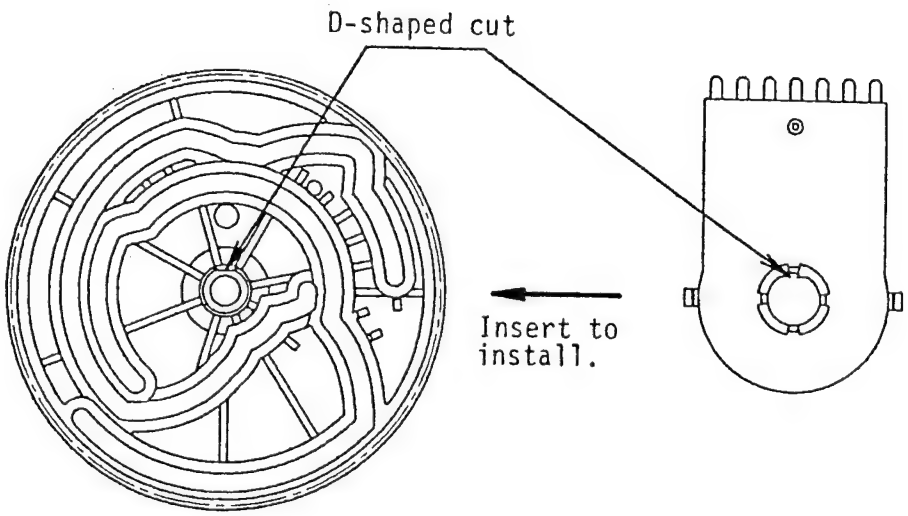


Figure 1-20. Cam Switch Alignment

The cam switch is installed with its D-shaped cut aligned with the D-shaped cut of the master cam. (The specially devised cam switch allows its alignment irrespective of the angle of rotation.)

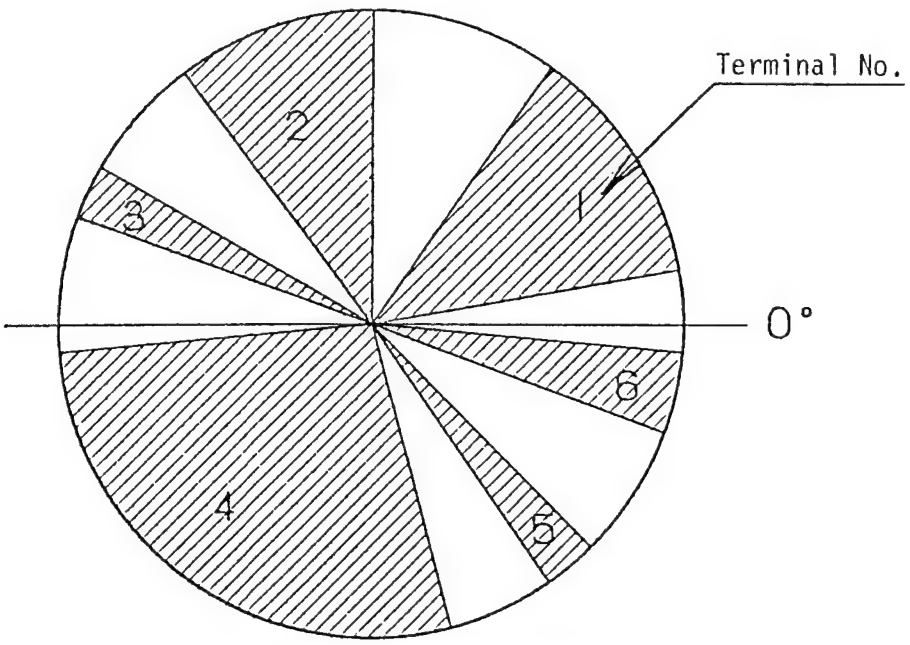


Figure 1-21. Structure of Cam Switch

The cam switch has an internal pattern as shown in Figure 1-21. and turns on the circuit at the shaded sectors. The system controller determines the mode of the mechanism by detecting turning on and off of the electric signal as the six shaded sectors make and break the circuit.

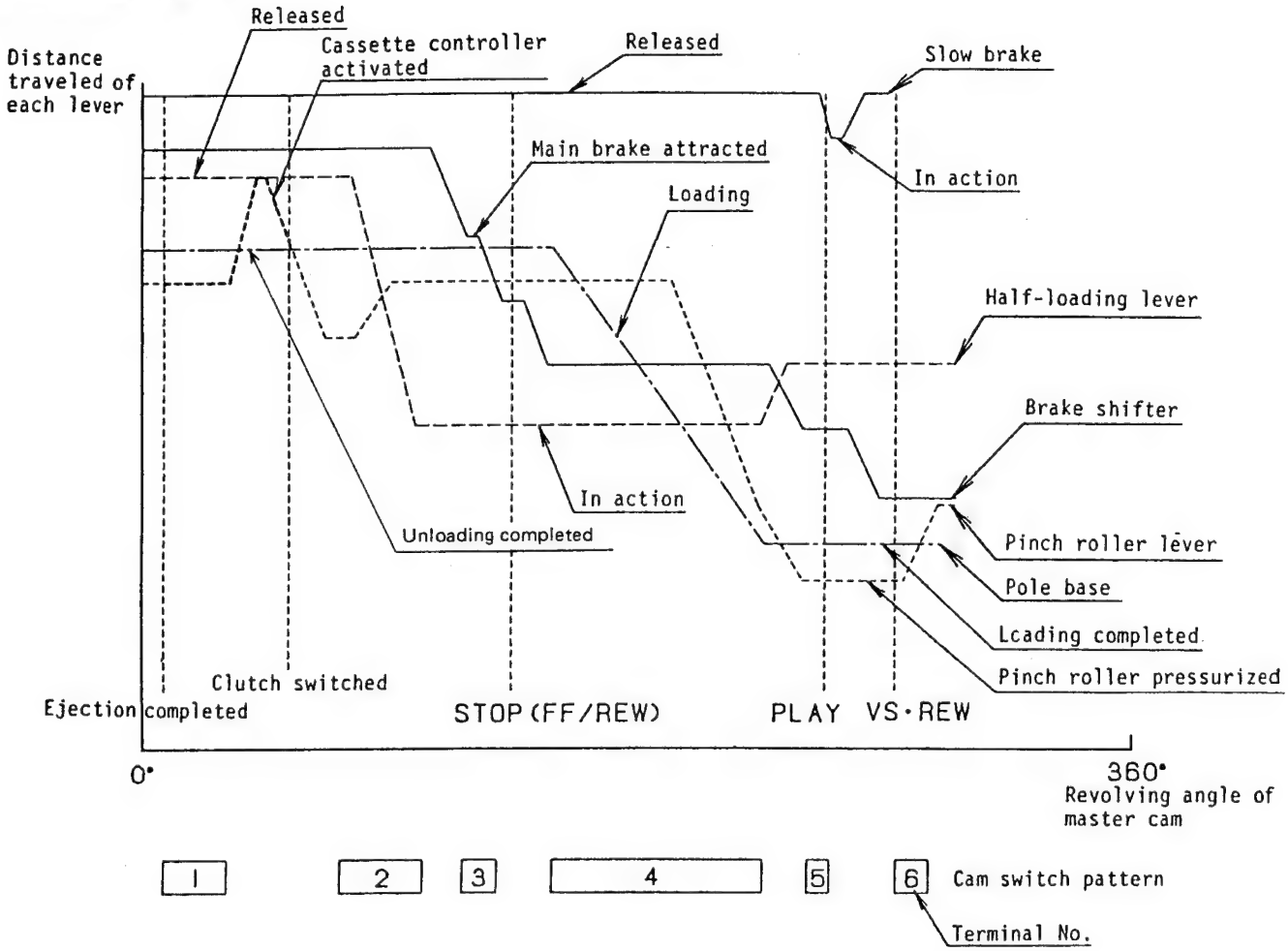


Figure 1-22. Relation between Cam Switch and Mechanism

Figure 1-22. shows the relation between the cam switch position and the actions of the individual components.

1-6. Cassette Control Mechanism

1) Cassette controller drive mechanism

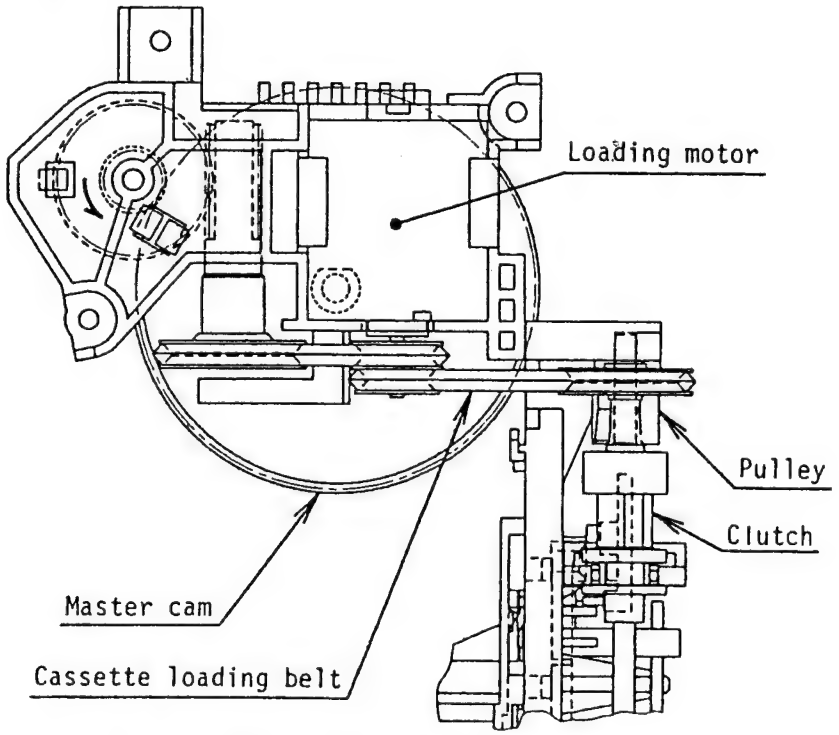


Figure 1-23. Cassette Controller Drive Mechanism

Feature

The driving force of the loading motor is always transmitted to the pulley of the cassette controller by the cassette loading belt as shown in Figure 1-23.

2) Configuration of cassette control mechanism

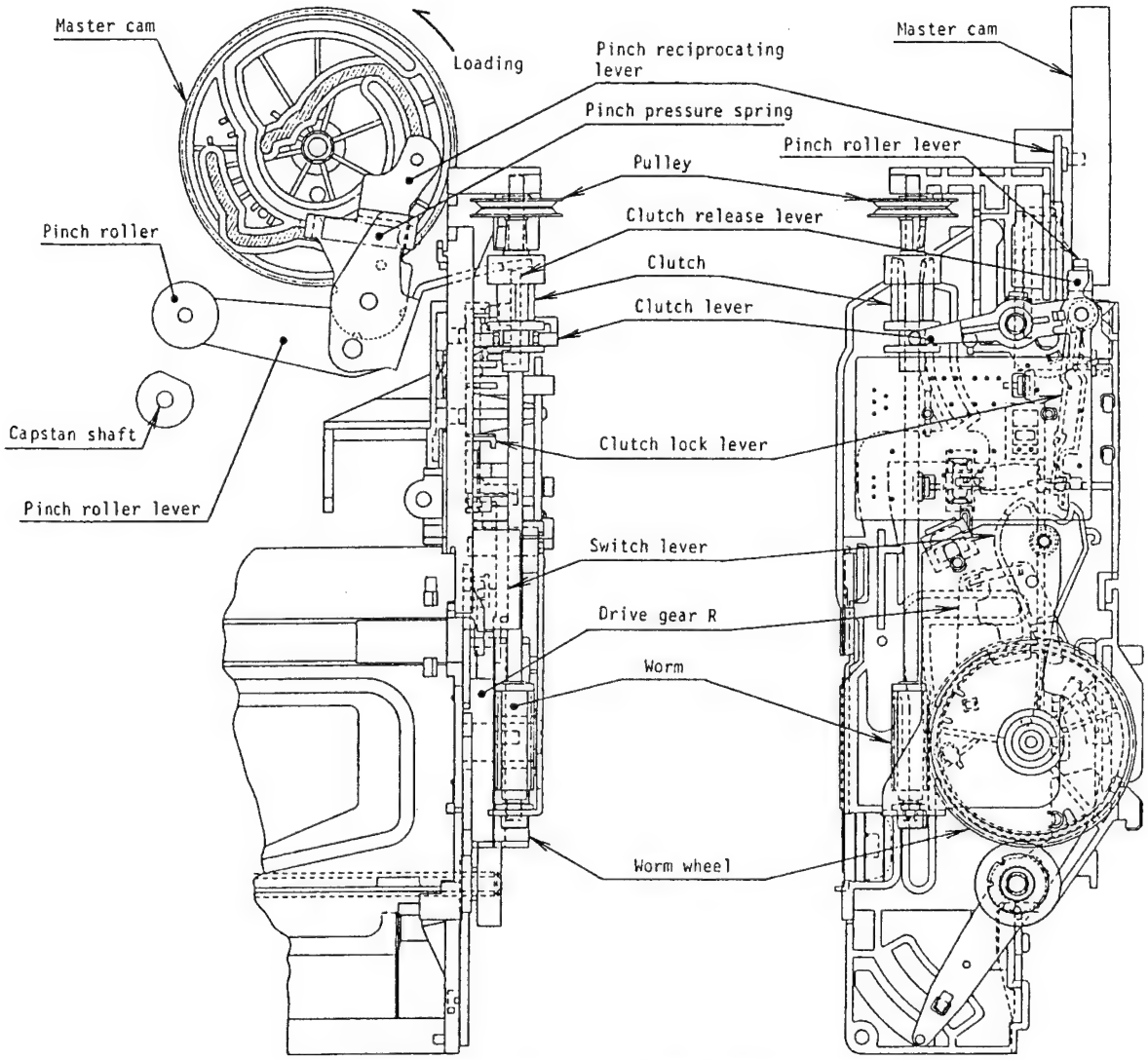


Figure 1-24. Relation between Pinch Roller Lever and Cassette Controller

The master cam acts on the pinch roller while the latter is positioned within the range where the pressurization of the pinch roller is not affected. The driving force of the loading motor is transmitted to the worm through the pulley.

1-7. Clutch Shifting Mechamism

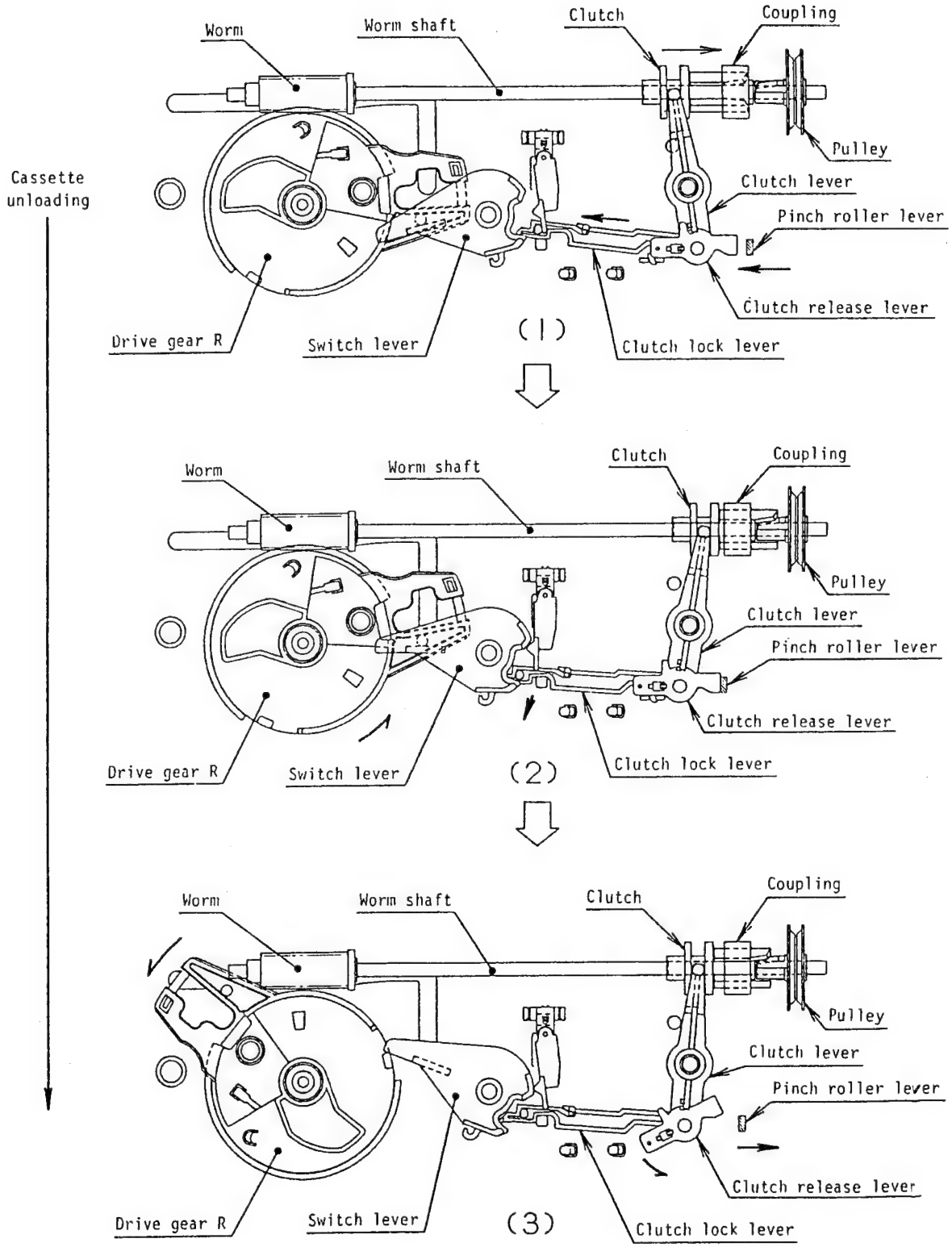


Figure 1-25. Cluch Shifting Sequence during Cassette Unloading

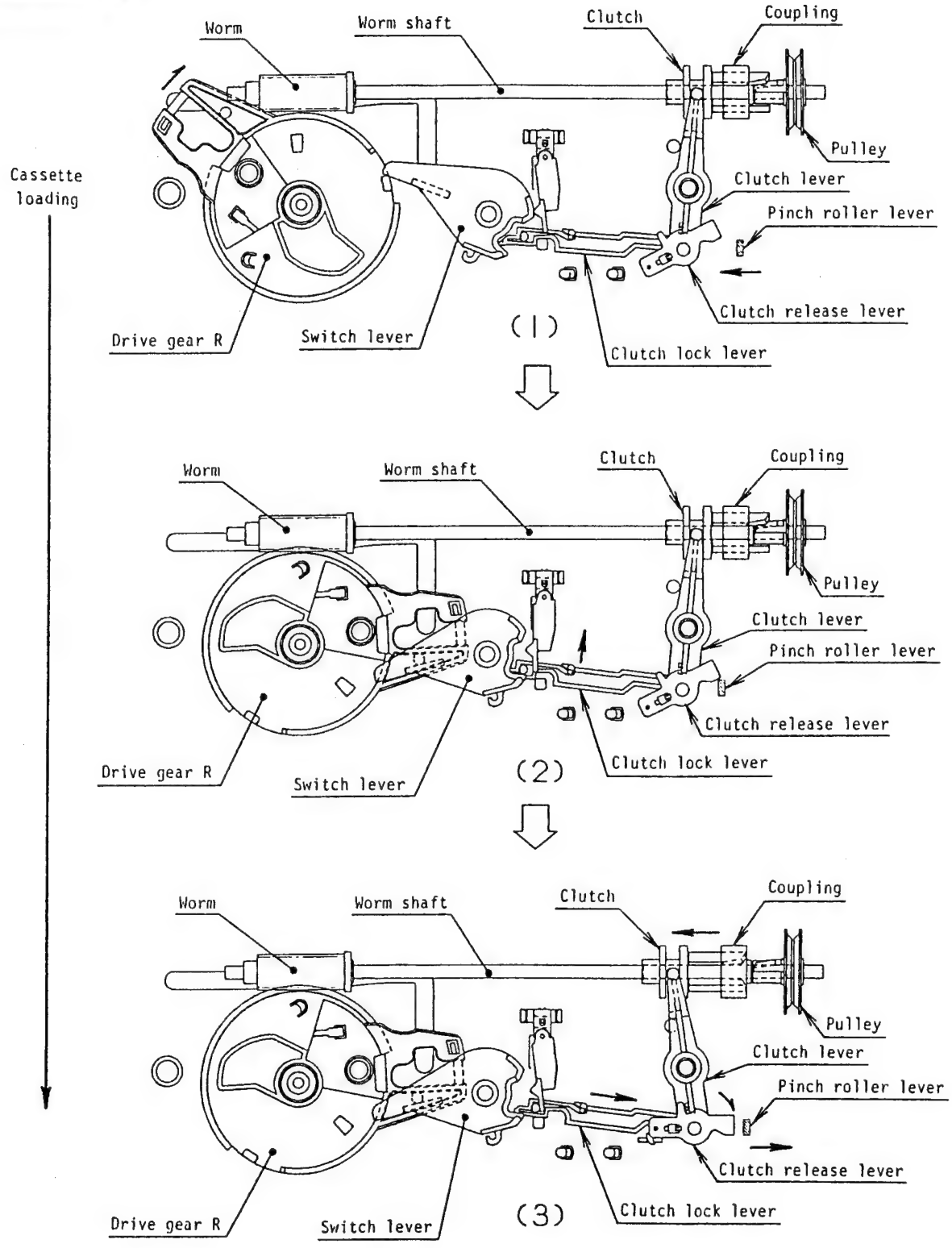


Figure 1-26. Clutch Shifting Sequence during Cassette Loading

1) Clutch Shifting Sequence during Cassette Unloading

The clutch is located as shown in Figure 1-25.(1) when the cassette has been loaded. In this condition the driving force of the pulley is not transmitted to the worm. As the pinch roller lever moves in the direction of arrow (a), the clutch, clutch lock lever and clutch release lever move in the directions (b), (c) and (d), respectively, bringing the positional relation in Figure 1-25.(2).
Now the driving force of the pulley is transmitted through the clutch and the coupling to the worm, which starts the drive gear R to unload the cassette.
At this time, the clutch lock lever is released from the switch lever and then fixed to the projection on the frame. By this the clutch is kept at a position even when the pinch roller lever comes to the position shown in Figure 1-25.(3).
When the drive gear R rotates to the position shown in Figure 1-25.(3), the switch lever turns on the switch and the motor stops. Now the cassette has been completely unloaded.

2) Clutch Shifting Sequence during Cassette Loading

Before a cassette is inserted, the clutch is positioned as shown in Figure 1-26.(1), where the driving force of the pulley is transmitted to the worm through the coupling.
When the cassette is inserted in this condition, the drive gear R starts turning by the reciprocating mechanism. Then the switch is released from the switch lever and the pulley starts turning to move the cassette in the loading direction. When the mechanism reaches a position just before completion of loading as shown in Figure 1-26.(2), the drive gear R forces the switch lever to rotate. Consequently, the clutch lock lever moves in the direction of arrow (e), releasing the clutch and turning on the switch at a time. Now the mechanism has loaded the cassette in position (Figure 1-26.(3)). The pulley remains running idle, and even when the loading motor is running, its force is not transmitted to the cassette controller.

2. SERVO CIRCUIT

Digital servo LSI (RH-IX0431GEZZ)

The digital servo LSI is of single-chip type and has the following functions.

- Drum speed and phase control.
- Capstan speed and phase control.
- Gain control for recording speeds (SP/LP).
- Automatic tape speed detection in playback mode.
- Head switching pulse generation in 1 PG system.
- X-value compensation in double-azimuth 4-head fine slow motion.
- Drum compensation and tracking shift in trick play mode (slow, still, frame advance, etc.).
- Amplification of record control signal.
- Others.

Below discussed are the names and functions of the pins of RH-IX0431GEZZ.

Pin No.	Name	Input/Output	Function
1	Vcc (for Analog circuit)	——	Power input terminal for analog amplifier (5 ± 0.5V).
2	Bias (+) (VREF (+))	Input	Reference bias voltage (2.5 V) settomg for analog amplifier and analog switch. Internally connected to the voltage follower input composed of C-MOS amplifier. 2.5 V reference voltage fed.
3	Bias (−) (VREF (−))	Output	Voltage follower output of the reference voltage fed at bias (+) (pin ②). Bias voltage of each amplifier inside the IC also connected to this pin.
4	Drum PG	Input	Negative drum phase generator pulse input. Threshold voltage is -70 mVp-p (TYP). Hysteresis is 60 mVp-p (TYP). (Positive square wave generated by the internal Schmitt amplifier)
5	Drum FG AMP	Input	Inverted input for inversion C-MOS amplifier of drum frequency generator. Bias preset at pin ② connected to this pin.
6	Drum FG AMP output	Output	Output terminal for inversion C-MOS amplifier of drum frequency generator.
7	Drum FG input	Input	Drum frequency generator Schmitt amplifier input terminal. Threshold voltage is 80 mVp-p (TYP). Hysteresis is 80 mVp-p (TYP).
8	Drum additional AMP output	Output	Additional amplifier output terminal for drum rotational control (C-MOS).
9	Drum additional AMP negative input	Input	Additional amplifier negative input terminal for drum rotational control (C-MOS).

Pin No.	Name	Input/Output	Function
10	Drum additional AMP positive input	Input	Addtional amplifier positive input terminal for drum rotational control (C-MOS).
11	Capstan FG input	Input	Capstan frequency generator Schmitt amplifier input terminal. Both threshold voltage and hysteresis are 80 mVp-p (TYP).
12	Capstan additional AMP output	Output	Additional amplifier output terminal for capstan rotational control (C-MOS).
13	Analog SW2	——	Built-in analog switch turns on at the servo serial data D18 = "1" and off at D18 = "0". Internally connected with capstan additional amplifier output to control the additional amplifier gain and to short-circuit the phase compensating capacitor. Slow, still, FF/REW and capstan stop modes brought on at D18 = "1".
14	Capstan additional AMP negative input	Input	Additional amplifier negative input terminalfor capstan rotational control (C-MOS).
15	Capstan additional AMP positive input	Input	Additional amplifier positive input terminal for capstan rotational control (C-MOS). (capstan speed and phase error voltages fed in)
16	GND (for Digital Circuit)	——	Ground for digital signal processing.
17	Drum phase error output (drum AFC)	Output	Drum phase error pulse width modulation (PWM) output terminal. Output at PWM repeated frequency $fsc/2^6 \fallingdotseq 69$ kHz. PWM duty stretched toward "H" due to phase delay. • Drum phase PWM output fixed at 50% duty if the drum frequency generator input frequency comes without about ±5% of the specified frequency.
18	Drum speed error output (drum AFC)	Output	Drum speed error PWM output terminal. Output at PWM repeated frequency $fsc/2^6 \fallingdotseq 69$ kHz. PWM duty stretched toward "H" due to speed (rpm) delay.
19	Capstan phase error output (capstan APC)	Output	Capstan phase error PWM output terminal. Output at PWM repeated frequency $fsc/2^6 \fallingdotseq 69$ kHz. PWM duty stretched toward "H" due to phase delay. Each capstan phase PWM output fixed at 50% duty in the following cases: 1) Drum frequency generator frequency out of about ±10% of the specified frequency.

<table>
<tr><th>Pin No.</th><th>Name</th><th>Input/Output</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td>2) Capstan frequency generator frequency out of about ±5% of the specified frequency.
3) No control pulse.
4) In serial data input mode for FF/REW, slow, short rewind (ASB*REV).</td></tr>
<tr><td>20</td><td>Analog SW 1</td><td>Output</td><td>Built-in analog switch turns on at the servo serial data D18 = ''1'' and off at D18 = ''0''. Bias voltage fed out of pin ③ when the switch turns on. Slow, still, FF/REW and capstan stop modes brought on at D18 = ''1''.</td></tr>
<tr><td>21</td><td>Capstan spped error output (capstan AFC)</td><td>Output</td><td>Capstan speed error PWM output terminal. Output at PWM repeated frequency fsc/2^6≒69 kHz. PWM duty stretched toward ''H'' due to speed down.</td></tr>
<tr><td>22</td><td>fsc (4.43 MHz) input</td><td>Input</td><td>4.43 MHz sub-carrier input terminal (C-MOS). Minimum operating compensation level at over 200 mVp-p. Inverting amplifier built-in.</td></tr>
<tr><td>23</td><td>LP mode (H)</td><td>Output</td><td rowspan="2">Tape speed detection logic output terminals for LP and SP modes (C-MCS output).
<table>
<tr><th>Output terminal \ Tape speed</th><th>LP</th><th>SP</th></tr>
<tr><td>LP (H) : PIN ㉓</td><td>H</td><td>L</td></tr>
<tr><td>SP (H) : PIN ㉔</td><td>L</td><td>H</td></tr>
</table></td></tr>
<tr><td>24</td><td>SP mode (H)</td><td>Output</td></tr>
<tr><td>25</td><td>Servo serial data input</td><td>Input</td><td rowspan="2">Servo LSI operation mode is set by these input terminals. 21-bit serial clock provided. Internal mode is set by identifying data bit ''1'' or ''0''; data bit ''1'' and ''0'' at serial data with ''H''and ''L'', respectively, at rising edge of serial clock. Serial transfer made with shift register. Internal transfer of 21-bit data made at serial data ''H'' at falling edge of serial clock. (See Servo Process Block Diagram (Fig. 3-19).)</td></tr>
<tr><td>26</td><td>Servo serial clock input</td><td>Input</td></tr>
<tr><td>27</td><td>PG mono-multi</td><td>Input</td><td>Mono-multi terminal for video/audio head switching pulse output timing. (Drum frequency generator and phase generator input signals, internally shaped into square wave, are used to generate phase generator mono-multi trigger pulse. By this pulse, the time constant of resistor and capacitor externally added is activated for time adjustment.)</td></tr>
</table>

Pin No.	Name	Input/Output	Function
28	Video H-SW-P output	Output	Video head switching pulse output terminal. 1. Double-azimuth 4-head switching: Video head switching pulse output timing in SP mode delayed by 2H (≒128 μsec.) compared to that in LP mode. (Actual video heads are set up by 2H difference.)
29	Hi-Fi H-SW-P output	Output	Hi-Fi head switching pulse output terminal. 1. 2-head switching: Head switching pulse output 90° behind the video head switching pulse. 2. Double-azimuth 4-head switching: Head switching pulse 60° behind the video head switching pulse. (Not used on the models of this series.)
30	Vertical sync. input	Input	Composite sync. input detected for vertical sync. by the internal logic. Vertical sync. is distinguished from horizontal sync. by the pulse width.
31	Tracking monitor output	Output	Internal tracking delay time point monitored for digital tracking. • Monitor output stretched toward "H" duty when tracking data (servo serial data D0 thru D5 — 6 bits — used) is raised. (The center value is 20.0 msec. inside the IC; 14.78 msec. at this pin, however.)
32	Control pulse duty detection output	Output	Control pulse duty identify output terminal. "L" level when control pulse "H" duty (time from positive pulse to negative pulse) is long (about 60%). "H" level when it is short (about 27.5%). Control pulse identify duty fixed at 40% (TYP) in the IC.
33	Control pulse Schmitt output	Output	Output terminal of the control signal that has been fed through Schmitt amplifier and converted into square wave. "H" level square wave made with positive pulse and "L" one with negative pulse. Internal control pulse square wave inverted and put out when tape travel is reversed.
34	Vcc (for Digital Circuit)	——	Supply voltage input terminal for digital circuit (5 ± 0.5 V).
35	$\overline{\text{TEST}}$	Input	"H" input to make the servo IC in TEST mode. Usually at "H" level.

<table>
<tr><th>Pin No.</th><th>Name</th><th>Input/Output</th><th>Function</th></tr>
<tr><td>36</td><td>Record control (−)</td><td>Output</td><td>Terminal to apply voltage to negative pole of control head in record mode.
(High impedance in playback mode)
• "L" level duty 27.5% at servo serial data D17 = "1" and 60% at D17 = "0".</td></tr>
<tr><td>37</td><td>Record control (+)</td><td>Output</td><td>Terminal to apply voltage to positive pole of control head in playback mode.
(High impedance in playback mode)
• "H" level duty 27.5% at servo serial data D17 = "1" and 60% at D17 = "0".</td></tr>
<tr><td>38</td><td>GND (for Analog Circuit)</td><td>——</td><td>Ground terminal for analog amplifier.</td></tr>
<tr><td>39</td><td>AMP (+)</td><td>Input</td><td>C-MOS amplifier positive input terminal.
Pulled with 37 kΩ (TYP) up to bias voltage at pin ③ inside the IC.</td></tr>
<tr><td>40</td><td>AMP (−)</td><td>Input</td><td>C-MOS amplifier negative input terminal.</td></tr>
<tr><td>41</td><td>AMP output</td><td>Output</td><td>C-MOS amplifier output terminal.
C-MOS amplifier composed at pins ㊴ and ㊵.
(Not used)</td></tr>
<tr><td>42</td><td>Control pulse Schmitt input</td><td>Input</td><td>Control pulse Schmitt amplifier input.
Threshold voltage of schmitt amplifier system is controlled by the servo serial data D19 "0", "1" and slow/still mode as shown below, and control pulse is given out from schmitt output (pin ㉝).
<table>
<tr><th>Mode / Spec</th><th>D19 "0"</th><th>D19 "1"</th><th>Slow/still</th></tr>
<tr><td>Hysteresis</td><td>330mVp-p</td><td>650mVp-p</td><td>45mVp-p</td></tr>
<tr><td>Center level</td><td>0 mV</td><td>0 mV</td><td>110 mV</td></tr>
</table>
Notes:
1) The hysteresis of both the positive and negative pulses of control pulse are used at D19 = "0" or "1", in any other modes than slow/still.
In slow/still mode, only the positive pulse peak is detected.
2) D19 = "1" is in FF/REW and video search modes.
3) D19 = "0" is in the other modes than above.</td></tr>
</table>

3. SYSTEM CONTROLLER LSI

- 2-head system: RH-iX0571GEZZ, RH-iX0577GEZZ
- 4-head system: RH-iX0572GEZZ, RH-iX0574GEZZ

3-1. System Controller Terminal Allocation.

I/O	Terminal Name	Name	No.		No.	Name	Terminal Name	I/O
O(C-MOS)	GND CTL	P20	64		1	Vcc	5V	
O(3S)	FV	P21	63		2	AVss	GND	
O(C-MOS)	FV CTL	P22	62		3	Vref	A/D REF, VOLTAGE	
O(C-MOS)	X2	P23	61		4	D-A	COUNTER F/R	O(C-MOS)
O(C-MOS)	CTL GAIN SW (L)	P24	60		5	PWM	BEEPER	O(N-CH)
O(3S)	DRUM CTL	P25	59		6	P63	AL PB (L)	O(N-CH)
O(3S)	CURRENT LMT	P26	58		7	P62	BIAS CTL (H)	O(N-CH)
O(3S)	CAPSTAN CTL	P27	57		8	P61	POWER CTL (L)	O(N-CH)
O(N-CH)	CAPSTAN RVS (H)	P00	56		9	P60	VCR (L)	O(N-CH)
O(N-CH)	CAPSTAN PU (L)	P01	55		10	AN7	CAM SW	I (A/D)
O(N-CH)	CAPSTAN UL (L)	P02	54		11	AN6	CASSETTE SW	I (A/D)
O(N-CH)	LOADING FWD CTL	P03	53		12	AN5	AUTO FUNCTION	I (A/D)
O(N-CH)	LOADING RVS CTL	P04	52		13	AN4	NC	I (A/D)
O(N-CH)	BRAKE SOLENOID	P05	51		14	AN3	FV M.M.	I (A/D)
O(N-CH)	SERVO S DATA	P06	50		15	AN2	SLOW/STILL TRK	I (A/D)
O(N-CH)	SERVO S CLOCK	P07	49		16	P41	SPEED DET	I
O(N-CH)	TRANSIT (H)	P10	48		17	P40	NC	O(N-CH)
O(N-CH)	H. AMP SW	P11	47		18	SRDY	S.T READY (L)	O(N-CH)
O(N-CH)	CHROMA ROTARY	P12	46		19	CLK	T.S CLOCK	I
O(N-CH)	SLOW/STILL (H)	P13	45		20	SOUT	S.T DATA	O(N-CH)
O(N-CH)	PB AUDIO (H)	P14	44		21	SIN	T.S DATA	I
O(N-CH)	HiFi CTL	P15	43		22	CNTR	SEARCH (L)	O(N-CH)
O(N-CH)	AUDIO MUTE (L)	P16	42		23	INT2	ENVELOPE DET (L)	I
O(N-CH)	EE (L)	P17	41		24	P31	ENVELOPE DET	I
I	SYNC DET (H)	P50	40		25	P30	H.SW.P	I
I	REEL SENSOR	P51	39		26	INT1	H.SW.P (L)	I
I	START SENSOR	P52	38		27	CNVss	GND	
I	END SENSOR	P53	37		28	ACL	ACL (L)	I
I	INDEX IN	P54	36		29	XIN	CLOCK IN	I
I	DEW SENSOR	P55	35		30	XOUT	CLOCK OUT	O
I	NC	P56	34		31	Ø	NC	O
I	PB CTL	P57	33		32	Vss	GND	

RH-iX0571GEZZ, RH-iX0572GEZZ, RH-iX0574GEZZ, RH-iX0577GEZZ

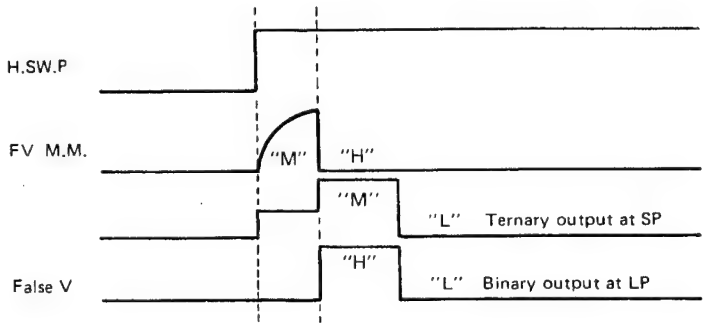
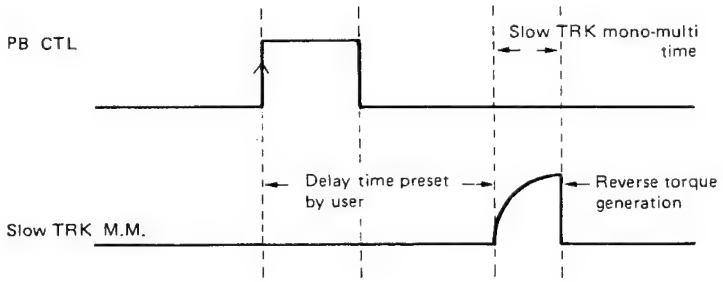
Figure 3-1. Bottom View

Note: On RH-iX0571GEZZ (for 2-head models) and RH-iX0577GEZZ (for 2-head LP models), pins 23, 24, 46 and 47 are not connected.

3-2. TERMINAL DESCRIPTION (2-/4-HEAD SYSTEM)

Pin No.	Control Signal	Specifications
1	5V	Vdd terminal
2	GND	AVss terminal (GND) To be connected to GND
3	A/D REF VOLTAGE	Reference voltage for A/D converting
4	COUNTER F/R	It is a control signal offering the tape running direction to the timer IC. (1) Counter CTL = "H" : Reverse turn Counter CTL = "L" : Positive turn (2) Other than the model below should be identical to the capstan motor direction. Namely, in case of capstan reverse turn- "H", counter CTL = "H" is applied. • Cue sound countermeasures for FF/REW-Stop, etc. (Idler neck swing) • Idler neck swing • Inversion brake time for VS release (3) In the mode below, the following are to be taken to adjust to the tape running direction. (For use of real time counter) • At loading ..... Counter CTL = "L" • Eject position/Stop position ..... Counter CTL = "L"
5	BEEPER	This output shows the time of confirmation sound output when the operating key is pressed. • Confirmation sound "ON time" = "H" • Confirmation sound "OFF time" = "L" **[System controller]** (1) The time of outputting a confirmation sound is 47 msec. (2) The timing of outputting a confirmation sound is to be at receiving of keys below. • Power key • REC key • TV/VCR key • Pause key • Eject key • REW key • Stop key • Slow key • FF key • Double speed key • PB key • At INDEX writing (optional writing) **[Timer]** (However, the confirmation sound output is only when the timer serial data takes buzzer request.) (1) The time of outputting a confirmation sound is 47 msec. and 1 sec. (2) To output the 47 msec. confirmation sound, it is done when 47 msec. short sound buzzer 1 is present with the timer serial data. (Refer to the timer ref. material for the operating key outputting a short sound buzzer request.) • For the time of confirmation sound, it is shorter than the above value at Slow/Still.
6	AL PB (L)	A signal to select REC mode with PB mode (1) In case of PB-system mode (PB, Still, Slow, VS-F/R, double speed) at PB. REC position, AL PB (L) = "L" is applied. (2) When the PB-system mode is released, it should be AL PB (L) = "H".

Pin No.	Control Signal	Specifications
7	BIAS CTL (H)	A signal to control start/end of recording of video/audio signal
8	POWER CTL (L)	A signal to control the power (supply) (controlling a driving-system power) (1) When the Power key is pressed at Power "OFF", it should be PCON (L)="L". However, in case of timer stand-by, the Power key should be in-effective. (2) When the Power key is pressed in ON mode, it should be PCON (L)="H". However, during mecha-operation, PCON (L)="L" is continued, and PCON (L)="H" is applied at the next mecha-position. • Stop position • Slider Up position (3) At timer stand-by, if the timer start data of timer serial data is detected, it should be PCON (L)="L", making REC display. (Timer recording start) (4) At timer stand-by, it should be PCON (L)="H". However, in VPS Interrupt mode, PCON (L)="L" is applied. (5) For driving of loading motor, cassette motor or capstan motor, if PCON (L)="H" is present, it should be made PCON (L)="L", and after driving, it is made PCON (L)="H". (6) In case of EE (L)="L" and PCON (L)="L", if weak electric field (L) input="L" continues for 30 min., it is automatically to be PCON (L)="H", allowing the mis-power-OFF preventive function to be effected.
9	VCR (L)	Control signal to switch on and off the signal to come to the RF converter. (1) Signal from the video tuner or playback signal from the video tape fed in with VCR (L) signal at "L". (2) Antenna input (VHF) signal fed through in with VCR (L) signal at "H". (3) VCR (L) signal at "H" with power control (L) signal at "H". (4) With power control (L) signal at "L", the TV/VCR selector key switches VCR (L) signal: • From "H" to "L". • From "L" to "H". (5) When the Stop key is pressed during playback mode, the following are obtained. i) If the VTR mode (L)="L" at output of playback screen, VTR mode (L)="L" is continued. ii) If the VTR mode (L)="H" at output of playback screen, VTR mode (L)="H" is continued.
10	CAM SW	
11	CASSETTE SW/REC TIP	This terminal has the A/D converting function of 6-resolution for analog voltage by the comparator (IC built-in) and D/A converter. (5 to 8)
12	AUTO FUNCTION	
13	NC	To be connected to Vdd or GND
14	FV M.M	It is intended to adjust the delay amount from the edge of H.SW.P to the generation of false vertical synchronous signal.

Pin No.	Control Signal	Specifications
		(1) Normally, "L" is outputted. (2) After detection of H.SW.P edge, the terminal is made to be "Z" (High impedance) and the mono-multi input taken. When recognized as "H", the mono-multi input is stopped and the terminal to be "L".  **Figure 3-2.**
15	SLOW/STILL TRK	It is intended to adjust the reverse torque generating timing at Slow/Frame advance. The preset is inputted to this terminal. (1) Normally, "L" is outputted. (2) At frame advance, when it detects the rising edge of PBCTL signal, it allows the delay time preset by user to pass by. Then, the terminal is selected to "Z" (High impedance) and such a mono-multi input started. When recognized as "H", the mono-multi input is stopped and the terminal to be "L".  **Figure 3-3.**
16	SPEED DET	Switches shown corresponding to A-F keys of D/A converting circuit

Key \ Input terminal	Mecha-posi. SW input	Speed detection input	Function selection input
A	CA SW	SP mode	Variable speed VS/Auto OFF
B	HF SW		Variable speed VS/Auto Repeat
C	FF SW	LP mode	Fixed Vs/Auto OFF
D	LD SW		Fixed VS/Auto Repeat
E	PB SW		Not used
F	PU SW		Not used
ALL SW "OFF"	SW OFF mode		Not used

Auto Power OFF: Auto power OFF function
Auto Repeat: Auto repeat playback function

Table 3-1.

Pin No.	Control Signal	Specifications

[Cassette controller SW]

Refer to cassette controller circuit. (Fig. 3-4)

SW \ Type	Cassette controller/Auto cassette controller	Specifications
A	Cassette controller SW (Insertion start detection)	ON: Cassette insertion start OFF: Other than above
B	Auto load SW (Cassette fit-in state detection)	ON: Cassette fit-in state OFF: Non-auto load cassette controller or cassette not fitted in
C	REC. Tip SW (Mis-erasing preventive tab detection)	ON: Preventive tab broken OFF: Preventive tab present
D	(CAS. Unit fit-in state detection)	• D-SW to be always "ON" at unit fit-in state • All SWs to be "OFF" without unit

Table 3-2.

D/A Converting circuit (Main body SW/CAM. SW/Function selecting SW/Cassette controller SW)

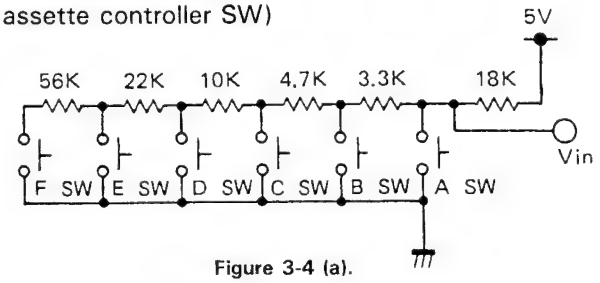
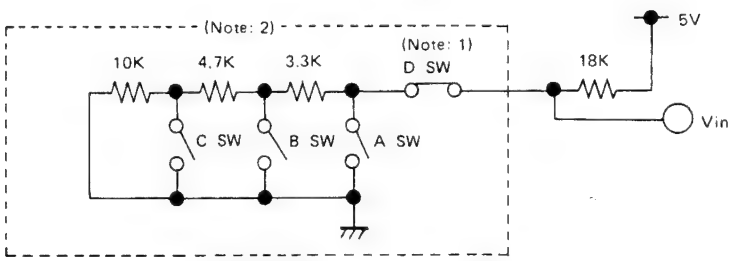


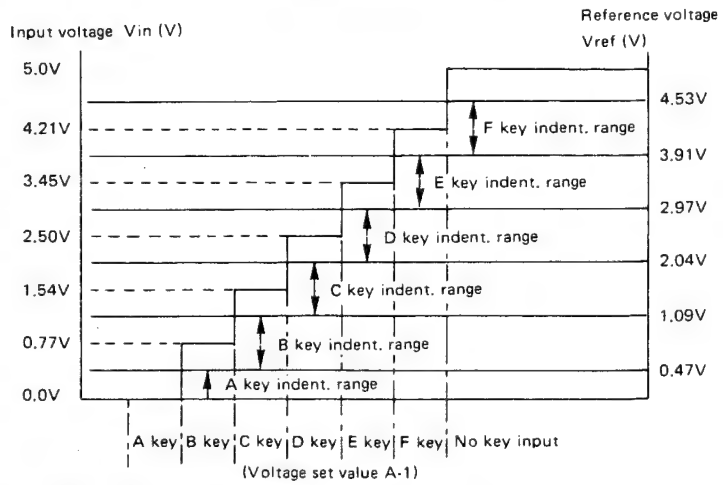
Figure 3-4 (a).



Cassette control circuit

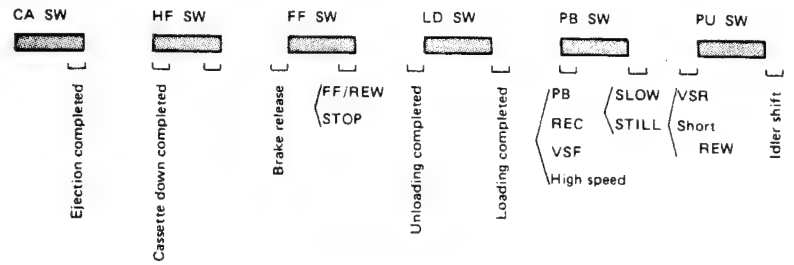
Note 1: The D switch is kept on all the time.
Note 2: The block framed with broken line is the cassette controller unit.

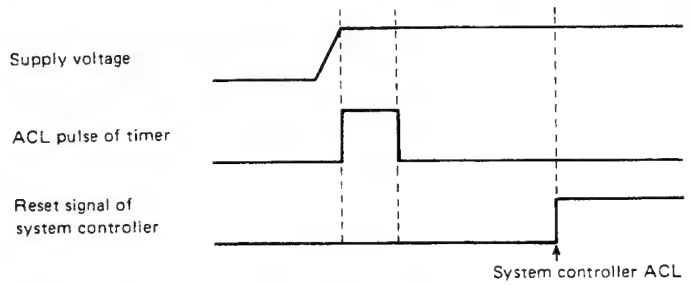
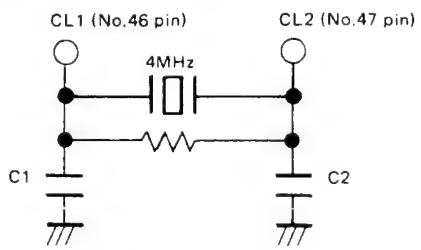
Figure 3-4 (b).



Input voltage (Vin) VS. reference voltage (Vref) with each switch.

Figure 3-4 (c).

Pin No.	Control Signal	Specifications
		 Figure 3-4 (d). **(CAM SW input)** • Refer to Fig. 3-4 for L-mecha. mecha-posi. and mode. **(Cassette control SW/REC Tip input)** • Timing of cassette insertion/Detection of REC. Tip state **(Cassette controller SW)** (1) SW A detects start of cassette insertion in slider UP condition. (2) SW B is intended for Auto load cassette controller and "ON" when the cassette is fitted in slider UP condition. For normal-type cassette controller, it is always "OFF". (3) SW D is conceptual and always "ON" when the CAS. unit is fitted in. **(REC Tip SW)** (1) It is "ON" at REC Tip broken and "OFF" at REC Tip present. (2) It takes Eject immediately, if the "REC/timer REC" mode is to be started at REC Tip broken. (Tab-broken cassette/Auto-Eject function) **(Speed detection input)** Input to detect a tape speed data of 4H/2H (1) Refer to the preceding para. of "A/D terminal description" for the relation between the recording mode and the voltage level to be inputted. (2) The data inputted is transferred to the timer IC as below. i) In Stop/REC mode, the data of speed detection input is made ineffective, and the data of recording mode selected by timer is made to be a serial signal, transferred and displayed. ii) At replay by PAL 2HEAD, the following codes are trasferred to the servo IC, instructed by "Audio 8CH spec. treatment" from the timer. • SP mode (Speed identification permitted) at Audio 8CH spec. treatment • SP fixed (Speed identification prohibited) at Audio 8CH spec. no-treatment
17	NC	NC Terminal: Terminal should to be open.
18	S.T READY (L)	Refer to Page 43.
19	T.S CLOCK	It is a control signal intended for serial transfer between the timer IC and the system controller IC. (1) It should be timer READY (L)="L" every 23.4 msec., and 8 bit x 5 byte transferring is taken. (2) For serial transfer, after timer READY (L)="L" has been made, the system controller serial data is set by trailing edge of serial clock from timer IC, and the timer serial data is inputted by rising edge of serial clock. And then, after input of 8 bit data, it should be timer READY (L)="H". (3) The time of timer READY (L)="H" is 1.3 msec. min. (4) For serial data, refer to page 42.
20	S.T DATA	
21	T.S DATA	

Pin No.	Control Signal	Specifications
22	SEARCH (L)	It is a control signal for selecting the gain of PB CTL signal. (1) In Video-Search F/R mode, it should be Search (L)="L".
23	ENVELOPE DET (L) (4-head only)	Reference signal for head amplifier/chroma rotary switching output. To be given out of the head amplifier module. (1) Used to control the head amplifier/chroma rotary switching output with the envelope comparison signal input as reference in each mode.
24	ENVELOPE DET (4-head only)	
25	H.SW.P.	Sensor input intended to detect the state of the drum to be rotated. (1) Head switching pulse to detect if the drum is running. (2) Drum remains running with drum speed-up at "Z" (high impedance) from loading start to unloading end. (3) If head switching pulse input stays in the state (2) above for 1.6 seconds, the head is stopped. It is the reference signal of FV output in trick mode (VSF/R, x 2, STILL/SLOW). (1) In trick mode, FV output is taken at the rising and trailing edges of HSW.P input (HSW.P). (2) A signal allowing start of frame advance.
26	H.SW.P.(L)	
27	GND	CNVss terminal (GND) To be connected to GND
28	ACL (L)	It is an initial resetting terminal of microcomputer, and allows the microcomputer to be initial-reset by applying the low voltage. In addition, with system controller reset signal, initial resetting is possible by connecting such a signal to the ACL terminal by the timer microcomputer. The timing of system controller reset signal on timer microcomputer is shown Fig. 3-5.  **Figure 3-5.**
29 30	CLOCK IN CLOCK OUT	The system clock generating circuit of microcomputer is built in, and the clock signal (4 MHz) is obtained by connecting the ceramic resonator shown Fig. 3-6.  **Figure 3-6.**
31	NC	NC terminal: Terminal should to be open.

Pin No.	Control Signal	Specifications
32	GND	Vss terminal (GND) To be connected to GND
33	PB CTL	Reference signal taking playback blue mute (1) Unless PB CTL rising edge can be detected during 120 msec. in PB mode, a blue mute request is taken to the timer IC. (2) Ref. signal for determining a time (61 ± 2 pulses) of "INDEX signal writing" (3) Detection signal for identifying a recorded tape (tab broken cassette) in Full Auto function • A signal causing reverse torque generation at frame advance
34	NC	To be connected to Vdd or GND.
35	DEW SENSOR	An input terminal to detect any dew situation (1) When the dew sensor is equal to "H", it identifies as dew situation and prohibits any mecha. actuation. However, the following keys should be effective regardless of dew situation. • Power • Eject/Insertion • TV/VTR (2) When the dew sensor is equal to "H", the mecha. position is moved to Eject position and done as follows: PCON (L)="L" ..... Drum mute (L)="H" PCON (L)="H" ..... Drum mute (L)="L" (3) When the dew sensor is equal to "L", the mecha. position is moved to Stop position.
36	INDEX IN	This input is to detect cue signal in INDEX mode. (1) "H" is inputted on cue recording section. (H to be 20 msec. min.) (2) By timer operation, Intro search (Interval search) and Index search are set. i) Setting of Intro search (Interval search) When the FF/REW key is pressed, it is shifted to Intro search. When the cue signal input "H" is detected during FF/REW mode, it comes to be PB mode during 7 sec. and is re-shifted to the FF/REW mode, continuing the cue signal input. ii) Release of Intro search (Interval search) When the mode is cleared by the timer, Intro search is released at once, continuing the current mode. When the mode key (STOP/FF/REW/PB/REC/SLOW/double speed key) is pressed during Intro search, the Intro search mode is released, allowing mode shifting. iii) Index search When the number of skips is set by Index search, the INDEX signal is detected, and then it is transmitted to the timer IC by the system controller SIO.
37	END SENSOR	A signal to detect a tape end (1) For detection of rising edge of end sensor input: i) In case of ON mode with cassette IN, auto-rewinding is taken. ii) During timer REC, Eject is taken after leader tape winding. (2) If in Stop mode, the tape is rewound and the leader tape wound until the end sensor input is "L". However, unless the end sensor input is "L" even after continuous rewinding for 5 sec., stop processing is taken.

Pin No.	Control Signal	Specifications
		(3) Cassette-down is judged by the end sensor input and the next start sensor input as follows: (Cassette controller down). ($\overline{\text{End sensor}}$) + ($\overline{\text{Start sensor}}$))="H" In such a case, cassette-down is recognized.
38	START SENSOR	A signal to detect a tape start (1) For detection of rising edge of start sensor input: i) In case of REW mode, stop processing is taken. ii) If during REC/PAUSE short rewinding, short rewinding is interrupted. (2) If is Stop mode, the tape is rapidly advanced and the leader tape wound until the start sensor input is "L". However, unless the start sensor input is "L" regardless of continous rapid-advance for 5 sec., stop processing is taken. (3) The start sensor input is utilized for cassette-down recognition. Refer to the paragraph of end sensor input.
39	REEL SENSOR	It is a sensor input intended to detect the reel stand situation when it is to be turned. (1) The situation subject to a reel stand turn is as follows: i) For loading completion: • PB • REC • VSF • VSR • Double-speed ii) For unloading completion: • FF • REW (2) In such conditions, unless the reel sensor input changes within the time of each mode shown below, stop processing is taken.

Mode	Shut-Off Time
SP-PB/SP-REC/FF/REW/Double-speed/1.5-time speed	5.0 sec.
LP-PB/LP-REC	10.0 sec.
Video Search Rewind/Video Search Reverse	1.2 sec.

Table 3-3.

		(3) For processing of tape slack detection, the edge of reel pulse to be inputted utilizing the reel sensor is to be counted.
40	$\overline{\text{SYNC DET}}$ (H)	It is an identifying terminal for weak electric field, being a signal to be outputted from the external Sync Det circuit for Hsync existence of input video signal. (1) For Hsync presence, it is weak electric field (L)="L". For Hsync not present, it is weak electric field (L)="H". (2) Input of weak electric field (L) is effective in case of EE (L)="H". (3) In case of EE (L)="L" (EE screen), if the weak electric field (L)="H" continues for 120 ms., it is to be a blue screen applied. (The timer IC takes OSD for application. However, that is only when the blue back ON/OFF SW is "ON".) (4) In Stop condition with PCON (L)="L", if the weak electric field (L)="H" continues for about 30 min., PCON (L)="H" is applied. (However, unless any execution instruction (T36) from timer IC is done, it is ineffective. At selection of Full Auto, T36="1".)

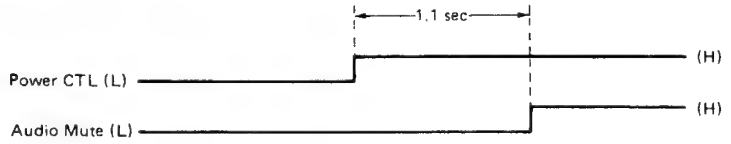
<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td>41</td><td>EE (L)</td><td>A signal of selecting between EE screen and playback screen
(1) The EE signal is intended to select the signal, i.e. the video/audio output is to be EE or PB, and thus in case of EE (L)="L" it selects to the signal (EE screen) to be transmitted from the tuner, and also at EE (L)="L" it selects to the signal (PB screen) to be transmitted from the video head.
(2) At PB. REC position, if it is PB-system mode and EE (L)="L", EE (L)="H" is applied about 1 sec. after positive turn of capstan motor.
(3) If the PB-system mode is released, it should be EE (L)="L".</td></tr>
<tr><td>42</td><td>AUDIO MUTE (L)</td><td>A signal to stop any audio output
(1) At Power CTL (L)="H", it should be Audio mute (L)="L" at any time.
(2) For Power "ON":
 

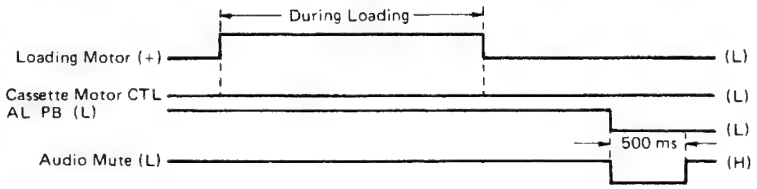
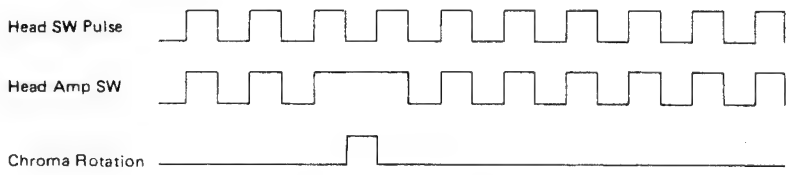
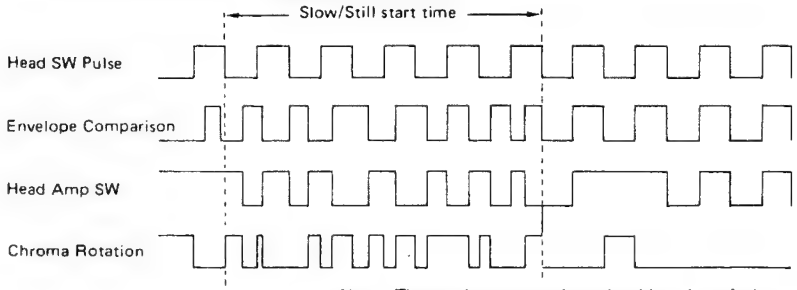
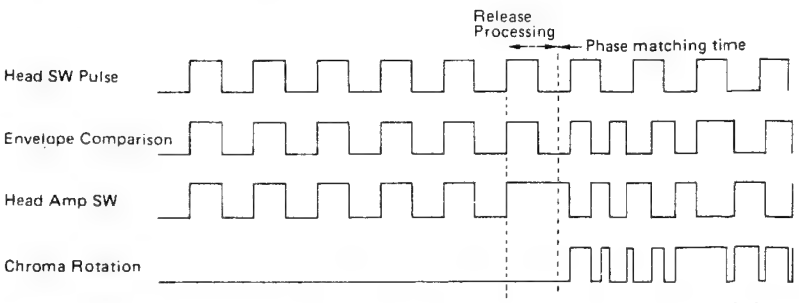
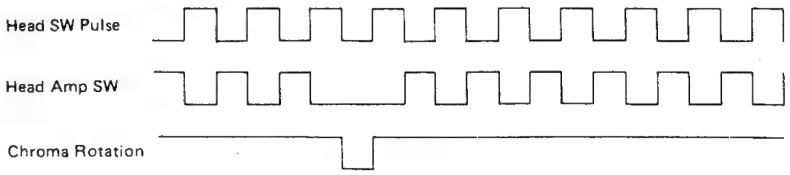
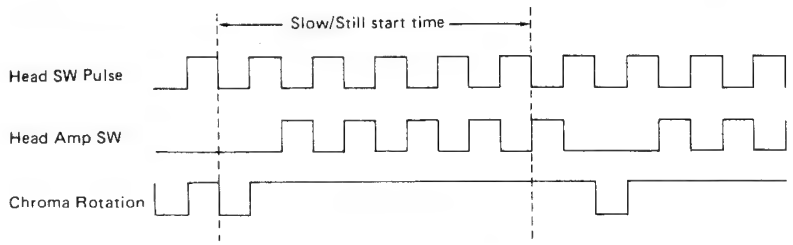
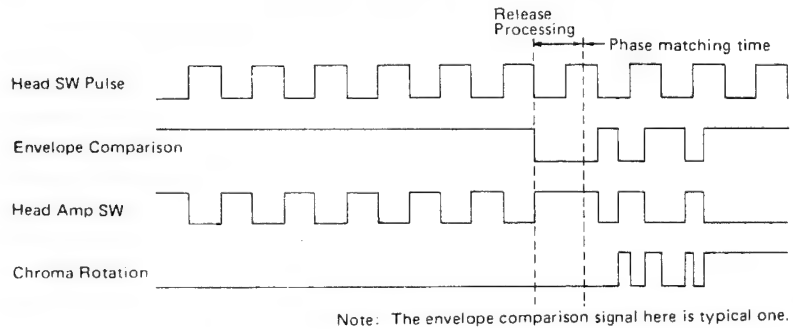
Figure 3-7.
(3) After PB loading end:
 

Figure 3-8.
(4) In PB mode, when the trick playback (Still, Slow, VSF, VSR & double speed) key is turned "ON", A mute (L)="L" is applied immediately, shifting to trick playback.
(5) When trick playback is released, it is moved to the mecha-posi. of PB mode, and then after about 1,000 ms, A mute (L)="H" is applied.
(6) When the PB mode is released with EE (L)="H" condition, A mute (L) should be ="L" for 500 msec.</td></tr>
<tr><td>43</td><td>HiFi CTL</td><td>Not used.</td></tr>
<tr><td>44</td><td>PB AUDIO (H)</td><td>Audio muting at PB Audio (H) → "H"
At EE (L) → "L"
<table><tr><th>Pin ⑩ $\overline{\text{SYNC DET}}$ (H)</th><th>PB AUDIO (H)</th></tr><tr><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td></tr></table>Table 3-4.
At EE (L) → "H"
<table><tr><th>Pin ⑫ FV CTL</th><th>PB AUDIO (H)</th></tr><tr><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td></tr></table>Table 3-5.</td></tr>
</table>

Pin No.	Control Signal	Specifications
45	SLOW/STILL (H)	"H" at Slow/Still Not used
46	CHROMA ROTARY (4-head only)	Terminal to select chroma. (1) Right channel: "H" (6° azimuth head side). (2) EXOR logic for head switching pulse and head amplifier switching signal.
47	H.AMP SW (4-head only)	Output to select between SP and LP heads. (1) SP mode: "H" LP mode: "L" (2) Head amplifier switching control signal at "L" in LP mode. (3) Inverted envelope comparison input signal (pin ㉔) to be outputted at VS-F/R in SP mode. (4) Signal to be outputted according to record mode of each step during slow/frame advance. **(SP mode)** • This signal remains in phase with head switching pulse during frame advance.  **Figure 3-9.** • This signal remains in anti-phase with envelope comparison signal at the start of slow/still mode.  Note: The envelope comparison signal here is typical one. **Figure 3-10.** • The envelope comparison signal is inverted after the slow/still mode is cleared.  Note: The envelope comparison signal here is typical one. **Figure 3-11.**

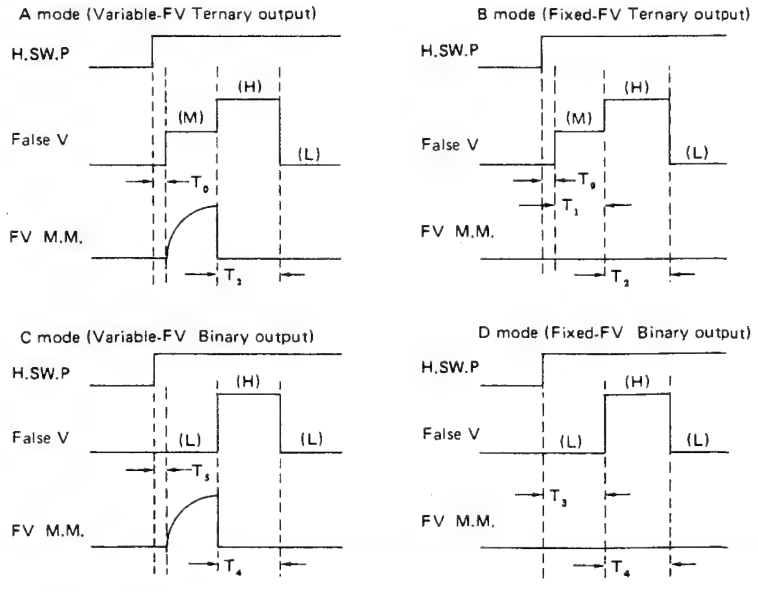
Pin No.	Control Signal	Specifications
		(LP mode) • This signal remains in anti-phase with head switching pulse during frame advance.  **Figure 3-12.** • The following timing is set up at the start of slow/still mode.  **Figure 3-13.** • The envelope comparison signal is inverted after the slow/still mode is cleared.  Note: The envelope comparison signal here is typical one. **Figure 3-14.**
48	TRANSIT (H)	When transferring from VS FWD and VS RVS modes to PB mode, it continues to be "H" for approx. 1,400 ms. Used to cope with colour dislocation
49	SERVO S. CLOCK	(1) The following are the method of data transfer to servo IC. The servo IC outputs the data of 21 bits to latch the servo/display serial data at rising edge of servo/display serial clock. Then, the serial output is completed by making servo/display serial data="H" at the final clock trailing edge. (2) For mode and data, refer to page 41.
50	SERVO S. DATA	
51	BRAKE SOLENOID	It is a signal for controlling the brake solenoid ON/OFF. (1) This signal is intended to control the brake solenoid ON/OFF, and in case of brake solenoid="H", the brake solenoid is made to be attracted. (2) When the REW key is pressed at FF.REW position, REW display is made, and it makes loading motor positive-turn CTL="L" and loading motor reverseturn="H", and after movement to brake release posi., brake solenoid="H" is applied.

<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td></td><td></td><td>(3) When the FF key is pressed at FF.REW position, FF display is made and then the same brake release processing as (2) is taken.
(4) If the cassette is already inserted and end sensor="H" or start sensor="H" is present, the same brake release processing as (2) is taken.
(5) In tape slack detection, it takes such a brake release processing identical to (2).
(6) When the REW key is pressed in case of EE (L)="H" at PB.REC posi., VSR display is made and brake solenoid="H" made, shifting to the VSR position. After shifting, brake solenoid="L" is applied.
Then, when the VSR mode is released, it makes brake solenoid="H" after stopping of tape running, and then upon shifting to PB.REC position, brake solenoid="H" is made.
(7) In the item of (2), (3) and (4) of capstan UL, brake solenoid="L" is made immediately before capstan UL (L)="H".
(8) It makes brake solenoid="L" immediately before release of FF/REW.</td></tr>
<tr><td>52</td><td>LOADING RVS CTL</td><td>(1) It is an output terminal for controlling the rotating direction of loading motor.</td></tr>
<tr><td>53</td><td>LOADING FWD CTL</td><td>Given below is the relevant combination.
<table>
<tr><th>Control Signal / Mode</th><th>Loading motor positive-turn CTL</th><th>Loading motor reverse-turn CTL</th></tr>
<tr><td>Loading motor Stop</td><td>L</td><td>L</td></tr>
<tr><td>Loading motor positive-turn</td><td>H</td><td>L</td></tr>
<tr><td>Loading motor reverse-tur</td><td>H</td><td>H</td></tr>
</table>
Table 3-6.
(2) For stopping condition of mecha. actuation:
• Loading motor positive-turn CTL="L"
• Loading motor reverse-turn CTL="L"
(3) The following functions are provided so as to prevent any overcurrent to the loading motor.
• 2.0 sec. shut-off at cassette controller actuation
• 7.0 sec. shut-off at loading arm actuation
(4) For shut-off, there should be loading motor positive-turn CTL="L" and loading motor reverse-turn CTL="L", and the loading motor is stopped, and then stoppage is continued at that position until the operating key input has any change.
However, if during positive-turn of cassette controller, the motor is reversely turned and the cassette is ejected at once.
(5) Actuation of cassette controller
i) In cassette insertion, unless the cassette controller moves to the cassette controller down-posi. within 2 sec., it is actuated in Eject direction immediately, and further if not moved to the cassette controller up-posi. within 2 sec., it takes shut-off.
ii) For cassette controller Eject, unless the cassette controller moves to the cassette controller up-posi. within 2 sec., it is actuated in the cassette inserting direction, and if not moved to the cassette controller down-posi. within 2 sec., it takes shut-off.</td></tr>
</table>

Pin No.	Control Signal	Specifications
54	CAPSTAN UL (L)	A signal to control a reel rotating torque (1) The capstan UL is a torque control voltage to be applied to the capstan motor, and to be "L" during unloading, at start of FF/REW or at tape-winding at Eject. i) If the Stop/FF/REW mode is obtained at PB. REC position, the loading motor is reversely turned, and after about 500 msec., capstan UL (L)="L" is made, and the capstan motor is reversely turned, stopping the capstan motor and capstan UL (L)="H" at brake release position. ii) When the FF key is pressed at FF. REW position, FF display is made, and after brake release, capstan UL (L)="L" is made, and the capstan motor is positive-turned and about 500 msec. later, capstan UL (L)="H" is applied. iii) When the REW key is pressed at FF. REC position, REW display is made, and after brake release, capstan UL (L)="H" is made, and the capstan motor is reversely turned and about 500 msec. later, capstan UL (L)="H" is applied. (2) In tape slack detection or leader tape-winding processing, for start of tape running, about 500 msec. capstan UL (L)="L" is to be applied. However, if the above processing is completed within 500 ms., capstan UL (L)="H" is made immediately. (3) Idler move at start of loading action. (4) Loose-tape winding processing upon cassette insertion (300 msec.) (5) Loose-tape winding processing during Eject actuation. (6) Countermeasure for tape slack at FF→Stop
55	CAPSTAN PU (L)	A signal to control a reel rotating torque (1) The capstan PU is a signal for controlling the torque control voltage of capstan motor, and outputs at the following timing. i) At transfer from PB. REC posi. to VSR posi. ii) At return from VSR posi. to PB/REC posi. iii) At idler move (Neck swing processing) iv) Idler move from tape-winding upon cassette insertion v) Idler move at REC—REC. Pause
56	CAPSTAN RVS (H)	It is a control signal for determining the rotating direction of capstan motor. (1) The mode is made by combining the terminal ⑤⑦ with forced acceleration.
57	CAPSTAN CTL (Forced acceleration)	It is an output accelerating (stopping) the rotation speed to the capstan motor. (1) For Slow/Still: i) At Still (still image) replay→Forced acceleration="H" ii) At Slow/Frame advance→Refer to a frame advance timing chart. 2) Other than Slow/Still i) Capstan motor rotation: Forced acceleration="Z" ii) Capstan motor stop: Forced acceleration="L"

Mode \ Control signal	Forced acceleration	Capstan motor reverse turn
Capstan motor stop	L	L
Capstan motor positive turn	H	L
Capstan motor reverse turn	H	H

Table 3-7.

Pin No.	Control Signal	Specifications
58	CURRENT LMT	It is an output offering a torque (current) limit to the capstan motor. (1) In case of Power CTL (L)="L", current limit="L" is outputted. (2) For Power CTL (L)="L": i) At Still (still image) replay→Current limit="Z" ii) At Slow/Frame advance→Refer to frame advance timing chart. iii) For other than above, current limit="H" is outputted.
59	DRUM CTL	This signal is to control the drum motor rotation, and stops the drum motor in case of drum mute (L)="L". (1) If PB, VSR, VSF, Still, Slow, double speed or REC display is obtained at FF/REW position, drum mute (L)="Z" is applied, and after 500 ms, loading is started. (2) If Stop, FF or REW is obtained at PB/REC position, unloading is started, and after completion, drum mute (L)="L" is applied. (3) Lateral swing acceleration at Slow/Still→Refer to a frame advance timing chart.
60	CTL GAIN SW (L)	It is a gain selecting output of PB-CTL amp. at FF/REW. (1) At FF/REW→CTL gain selecting CTL="H" output Other than above→CTL gain selecting CTL="L" output
61	X2 (H)	At double speed → "H" Not used
62	FV CTL	It is a control signal for APC correction of drum in trick mode. (1) In case of trick="H", drum correction is done. (2) At VS-F/R, double speed, slow & Still mode, trick="H" is made. (3) The timing of trick="L" is to be 1 sec. after phasing term after PB mode shifting.
63	FV	In trick mode (VS-F/R), it generates FV/FH and applies the synchronization. (1) Such a FV is generated in VS-F/R mode, mecha. shift time of PB→VS-R, mecha. shift time at VS-R release, mode holding time of VS-F/R release Slow/Still, and in the case of Head 2 giving no double speed. (2) The generation timing waveform is as shown below. (Note: H.SW.P applies to both rising and trailing.)  Note) M: High impedance Figure 3-15.

<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td></td><td></td><td>(3) Modes and output waveforms are listed below
<table>
<tr><th rowspan="2">Mode</th><th rowspan="2">Recording Mode</th><th colspan="2">Head SW Pulse</th></tr>
<tr><th>Rising</th><th>Trailing</th></tr>
<tr><td rowspan="3">VS-Forward/Reverse</td><td>2-head (SP)</td><td>D mode</td><td>D mode</td></tr>
<tr><td rowspan="2">4-head (SP)
(LP)</td><td>B mode</td><td>B mode</td></tr>
<tr><td>D mode</td><td>D mode</td></tr>
<tr><td rowspan="3">Still/Slow</td><td>2-head (SP)</td><td>D mode</td><td>C mode</td></tr>
<tr><td rowspan="2">4-head (SP)
(LP)</td><td>A mode</td><td>B mode</td></tr>
<tr><td>D mode</td><td>C mode</td></tr>
<tr><td rowspan="3">Double Speed</td><td>2-head (SP)</td><td>B mode</td><td>A mode</td></tr>
<tr><td rowspan="2">4-head (SP)
(LP)</td><td>A mode</td><td>B mode</td></tr>
<tr><td>D mode</td><td>C mode</td></tr>
</table>
Table 3-8.</td></tr>
<tr><td>64</td><td>GND CTL</td><td>It controls the (−) terminal of CTL head.
(1) 100 ms after bias CTL (L)="L", it should be GND CTL="L". (At REC)
(2) It should be bias CTL (H)="H", together with GND CTL="H".
(3) Normally, it should be "H".</td></tr>
</table>

3-3. Data Transmission Specification of Mechanism Controller Corresponding to Serial Mode Servo

- Data is transmitted with the following format.

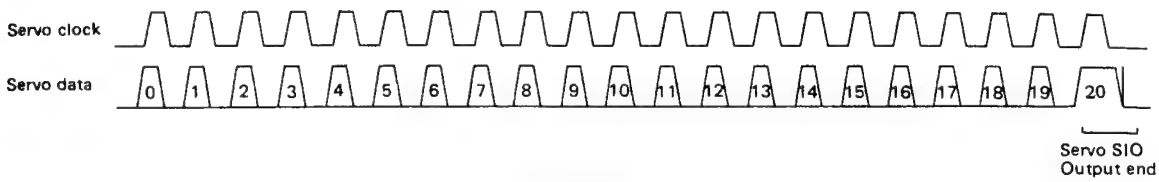


Figure 3-16.

(1) 21 bit data is outputted to the servo IC through the 2-line system consisting of servo clock (SCK) and servo data (SI).
(2) The servo data latches at the tail edge of servo clock. Servo SIO ends when the servo data is set to "H" at the servo clock tail.

1. Relation between Modes and Service Data

(The servo IC corresponds to RH-IX0431GEZZ)

Mode	Serial Data																
	0~5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
POWER OFF	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Serial transmission stop
POWER ON STOP	*1)	1	1	0	1	1	0	0	1	*2)		1	0	1	0	0	(FF2)
For 2.0S after FF start	*1)	1	1	0	1	1	0	0	0	*2)		1	0	0	1	0	(FF1)
FF subsequent	*1)	1	1	0	1	1	0	0	1	*2)		1	0	0	1	0	(FF2)
For 2.0S after REW start	*1)	1	1	1	1	1	0	0	0	*2)		1	0	0	1	0	(REW1)
REW subsequent	*1)	1	1	1	1	1	0	0	1	*2)		1	0	0	1	0	(REW2)
PB SP mode	*1)	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	(PB)
LP mode	*1)	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	(PB)
SP fixed mode	*1)	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	(PB)
VSF (M)	*1)	1	1	0	1	0	0	0	0	*2)		1	0	0	1	0	(SER2) SP: *5, LP: *5
(H)	*1)	1	1	0	1	0	0	1	0	*2)		1	0	0	1	0	(SER3) SP: *7, LP: *7
VSR (M)	*1)	1	1	1	1	0	0	0	0	*2)		1	0	0	1	0	(SER2/R) SP: *5, LP: *5
(H)	*1)	1	1	1	1	0	0	1	0	*2)		1	0	0	1	0	(SER3/R) SP: *7, LP: *7
SLOW	*1)	1	1	0	1	1	1	0	0	1	1	1	0	1	0	0	(SLOW)
STILL	*1)	1	1	0	0	0	0	0	0	1	1	1	0	1	0	0	(SLOW)
High speed	*1)	1	1	0	0	1	1	0	0	*2)		1	0	0	0	0	(*2)
REC SP mode	*1)	0	0	0	0	0	0	0	0	1	0	1	*3)	0	0	0	(REC)
LP mode	*1)	0	0	0	0	0	0	0	0	0	1	1	*3)	0	0	0	(REC)
SP fixed mode	*1)	0	0	0	0	0	0	0	0	0	0	1	*3)	0	0	0	(REC)
REC/pause	*1)	0	1	0	0	0	0	0	0	*2)		1	0	1	0	0	(REC · ASB)
Loading	*1)	0	1	0	0	0	0	0	0	*2)		1	0	1	0	0	(REC · ASB)
Unloading	*1)	1	1	0	1	1	0	0	1	*2)		1	0	0	0	0	(FF2)
Short loading	*1)	1	1	0	1	0	0	0	0	*2)		1	0	0	1	0	(SER1) / (*2)
Short unloading	*1)	1	1	0	0	0	0	0	0	*2)		1	0	1	0	0	(PB)
Trick cancel	*1)	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	(PB)
Short rewinding	*1)	0	1	0	0	0	0	0	0	*2)		1	0	0	0	0	(REC · ASB)
Phase matching	*1)	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	(REC · ASB)

Note *1 : Tracking delay time
D0 to D5 = "1 0 0 0 0 0" only in REC mode
In other modes the preceding data remains.

Note *2 : SP : 1 0
LP : 0 1
SP fixed : 0 0
Holding : 1 1

Note *3 : Only when writing the VISS signal: "1"
In other cases: "0"

Table 3-9.

2. Serial data D0 to D5

Serial Data						Tracking Delay time (msec)
0	1	2	3	4	5	
0	0	0	0	0	0	5.22
		↓				↓
0	1	1	1	0	1	18.62
		↓				↓
1	0	0	0	0	0	20.00
		↓				↓
1	1	1	0	1	0	32.01
		↓				↓
1	1	1	1	1	1	34.32

Note: The output from pin (31) of the servo IC (RH-IX0431GEZZ) is delayed by 5.22 msec.

Table 3-10.

3. Serial data D14 to D15

Serial Data		Speed Data
14	15	
1	0	SP
0	1	LP
0	0	SP fixed
1	1	Holding

Table 3-11.

4. Serial data D16 to D20

D16	Head Selection
0	D/A 4 Head
1	2 Head

D17	REC / DUTY Selection
0	REC · CTL 27.5%
1	REC · CTL 60 %

D18	CAP / SERVO SW
0	ANALOG SW ON
1	ANALOG SW OFF

D19	Hysteresis Width
0	300mVpp
1	600mVpp

D20	REC / CTL Selection
0	High-Z
1	GND

Table 3-12.

3-4. Serial Transmission Format between System Controller and Timer

1. Format of Data Transmitted from System Controller to Timer

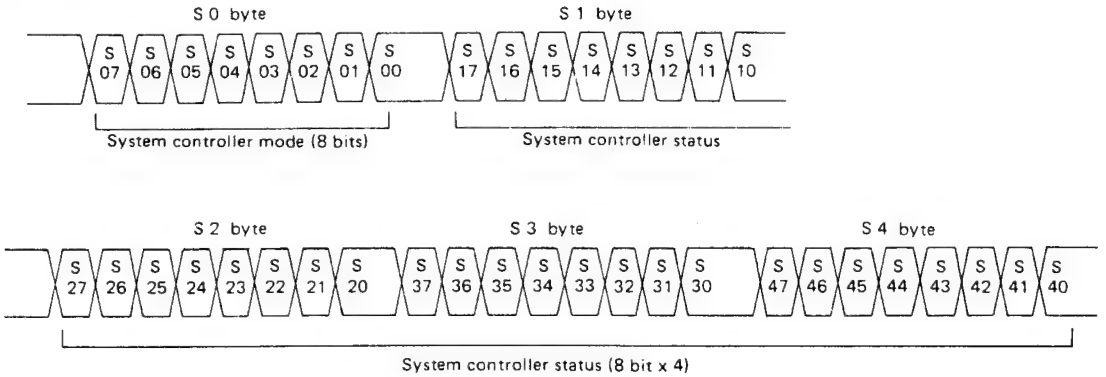


Figure 3-17.

(1) 5-byte data is transmitted by one transmission sequence.
(2) The S0 byte is arranged so that 8 bits compose one system controller mode data.
(3) The system controller mode is the system controller operation modes.
(4) The S1, S2, S3 and S4 bytes are 8 bite data which are used as system controller status data.
(5) The content of system controller status is represented the status of pertinent sensor by each bit.
(6) The timer makes the data valid when the same data is received twice successively (for S0, S1, S2, S3, S4).

2. Format of Data Transmitted from Timer to System Controller

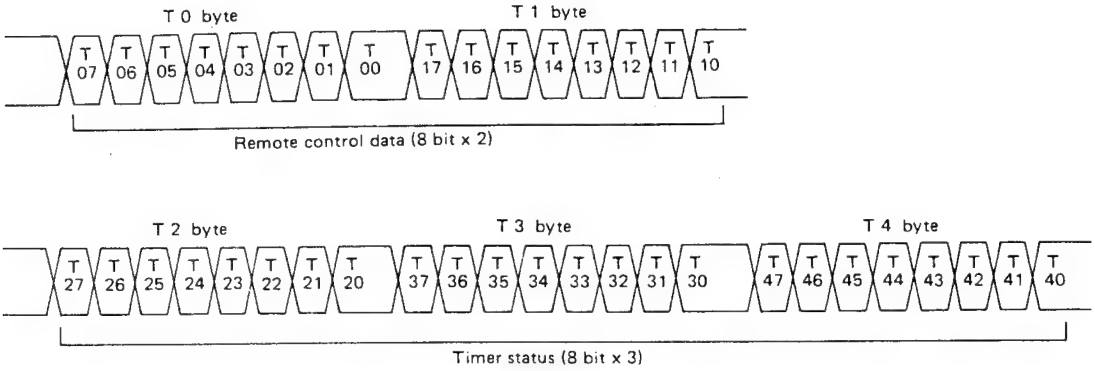


Figure 3-18.

(1) 5-byte data is transmitted by one transmission sequence.
(2) T0 byte and T1 byte are 8 bit data which are used as remote control data.
(3) The remote control data and they are determined by the content of control signals from the optical remote control and timer.
(4) The T0 byte and T1 byte have always the same data content.
(5) The system controller makes the remote control data valid if the T0 byte and T1 byte match with each other.
(6) The T2, T3 and T4 bytes are time master status data. The timer status consists of 8-bit flag it represents the timer status.
(7) The system controller makes the timer status data valid when the same timer status data is received twice successively.

VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

Servo Process Block Diagram

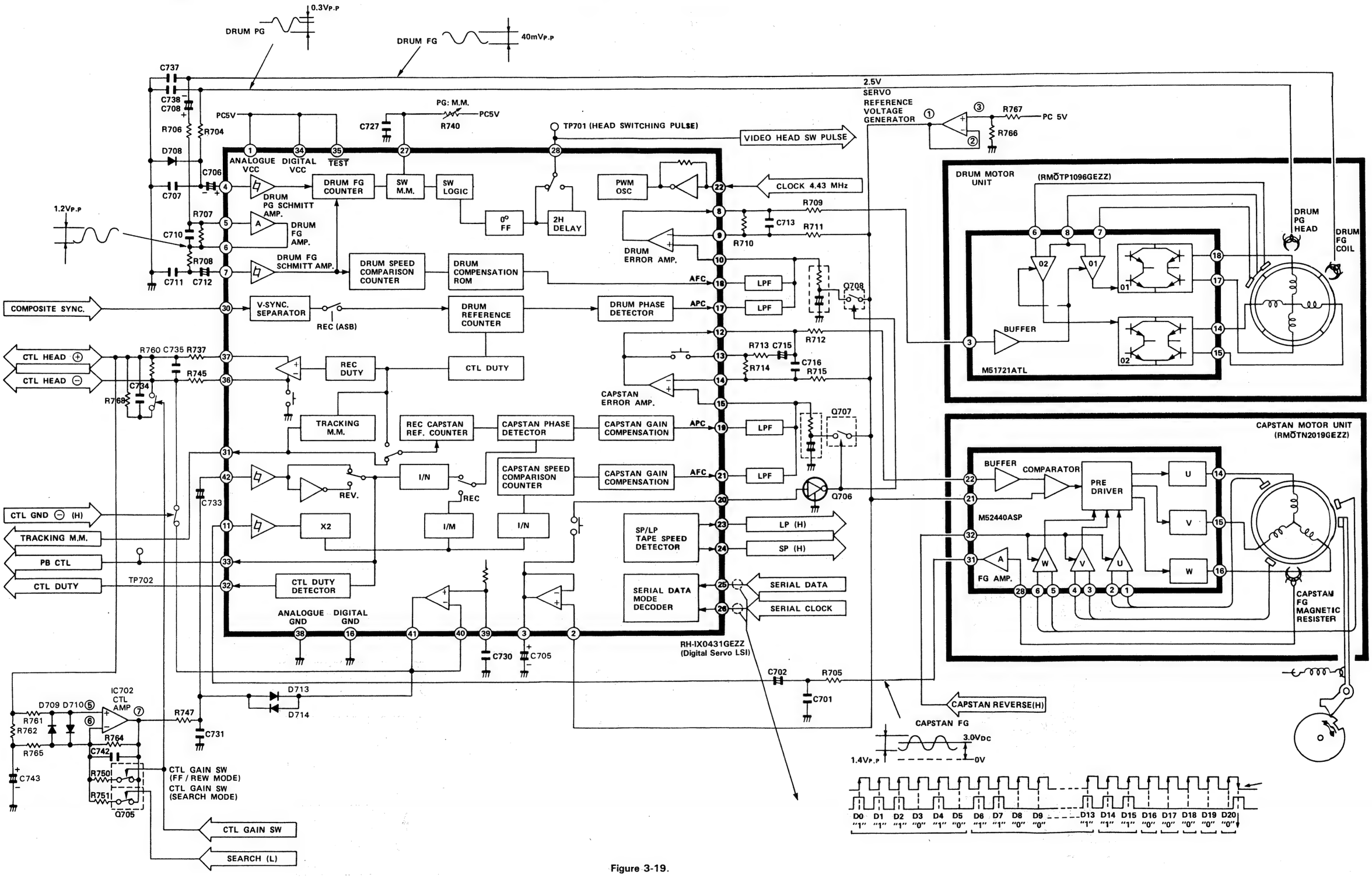


Figure 3-19.

VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

System Controller Block Diagram

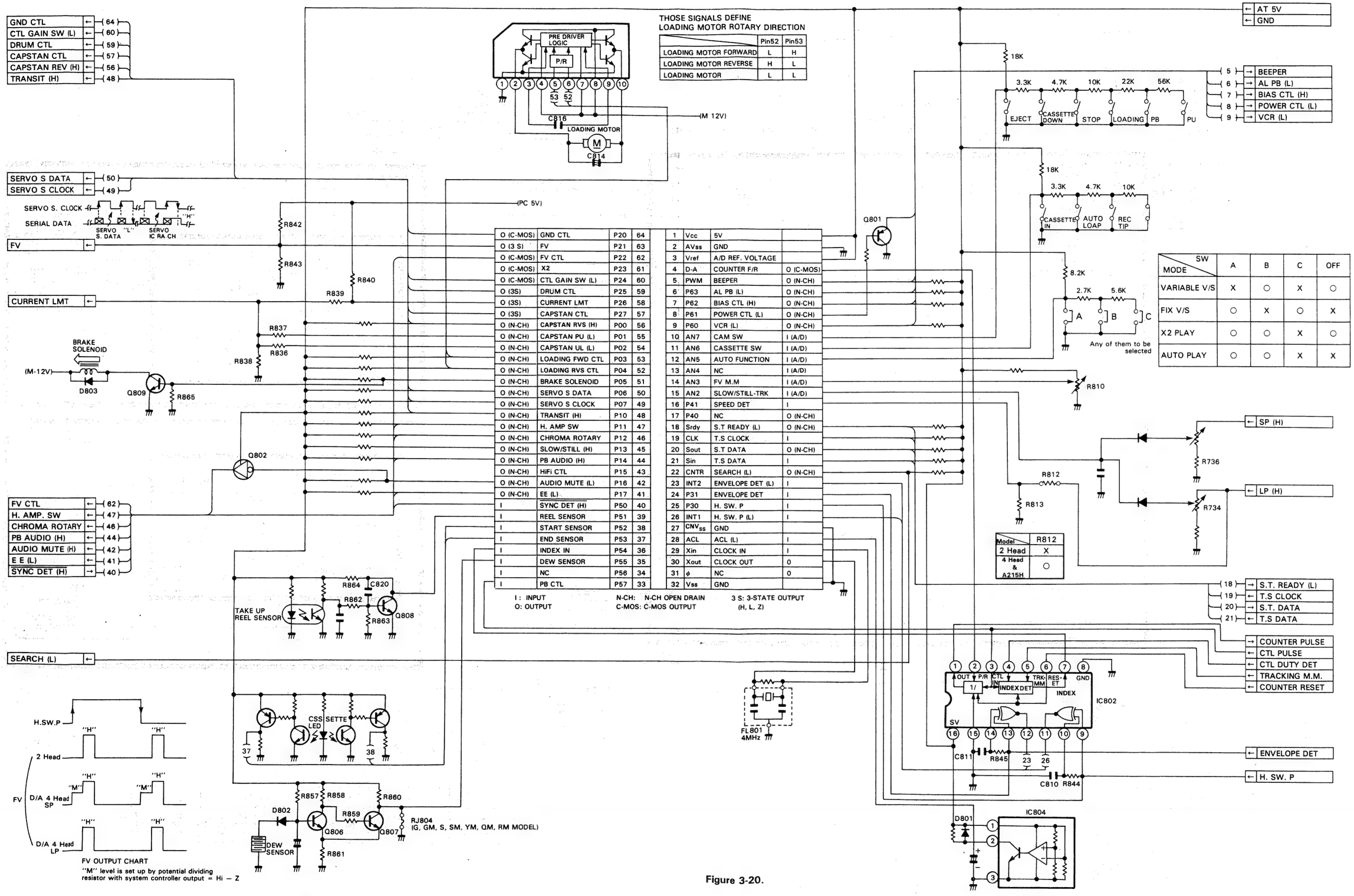


Figure 3-20.

4. TIMING CHART

Slow/Still Frame Advance Timing Chart (2-head system)

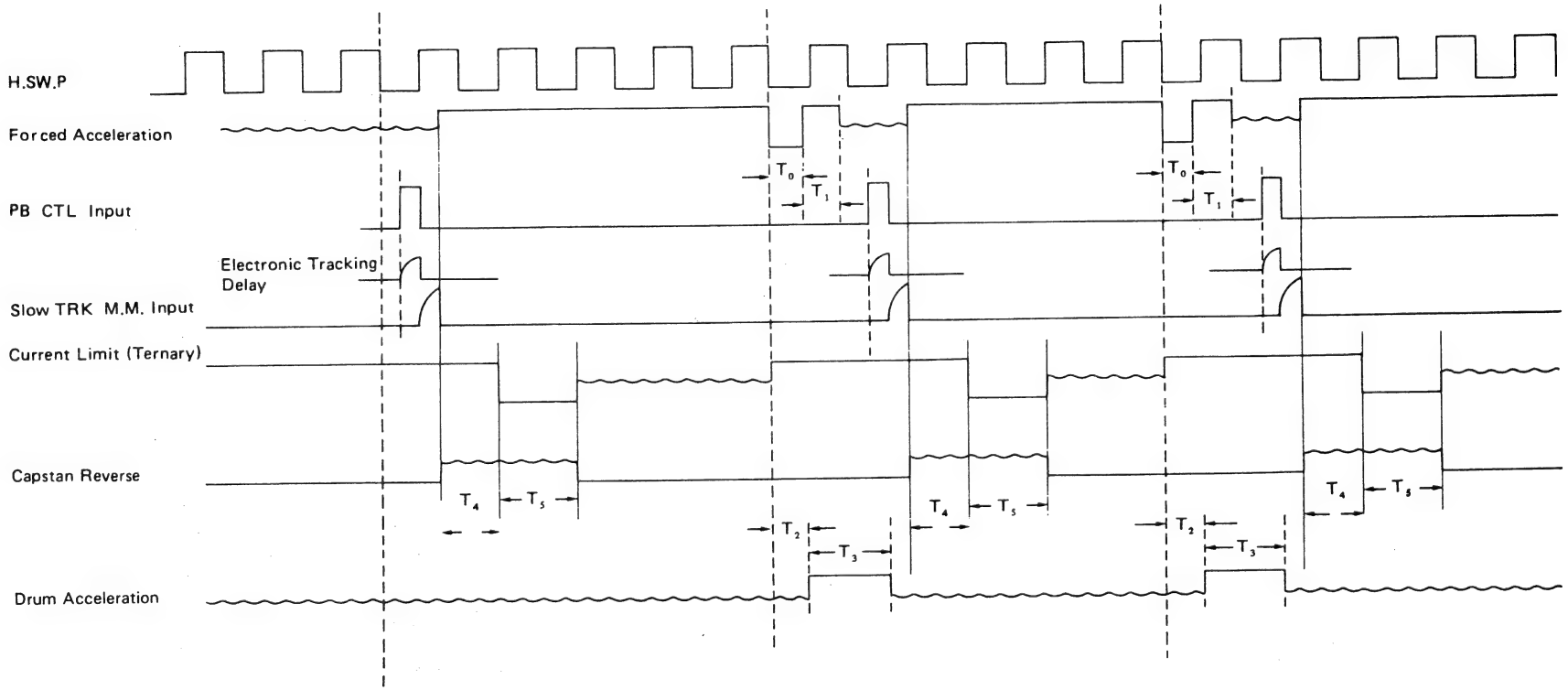


Figure 4-1.

Shift to REC/STOP mode when the Slow/Still mode is cleared (2-head system)

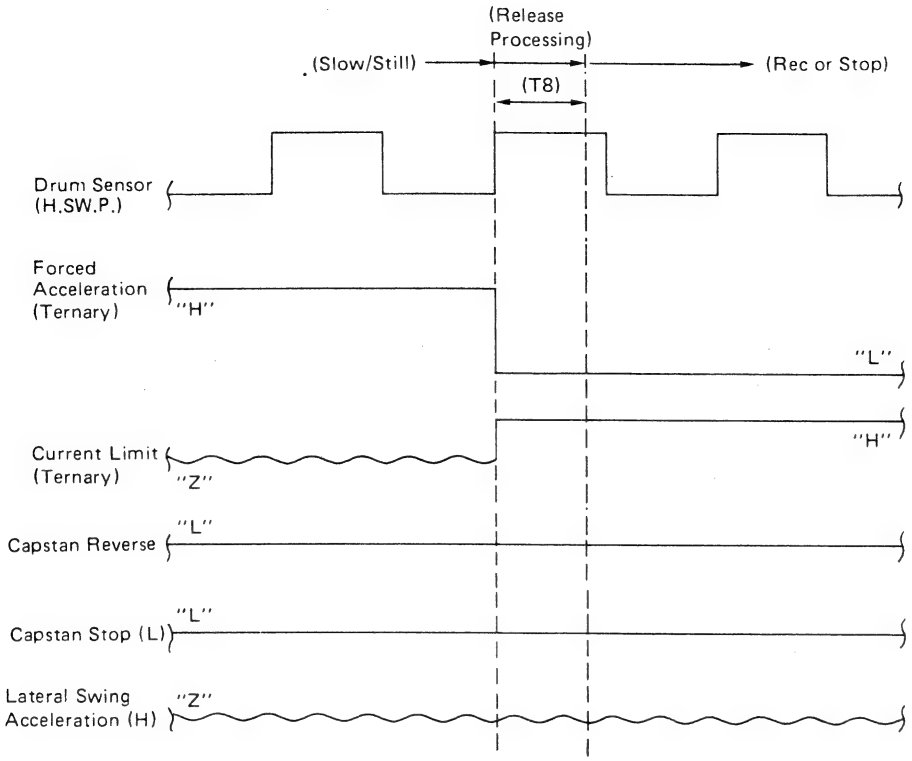


Figure 4-2.

Shift to PB mode when the Slow/Still mode is cleared (2-head system)

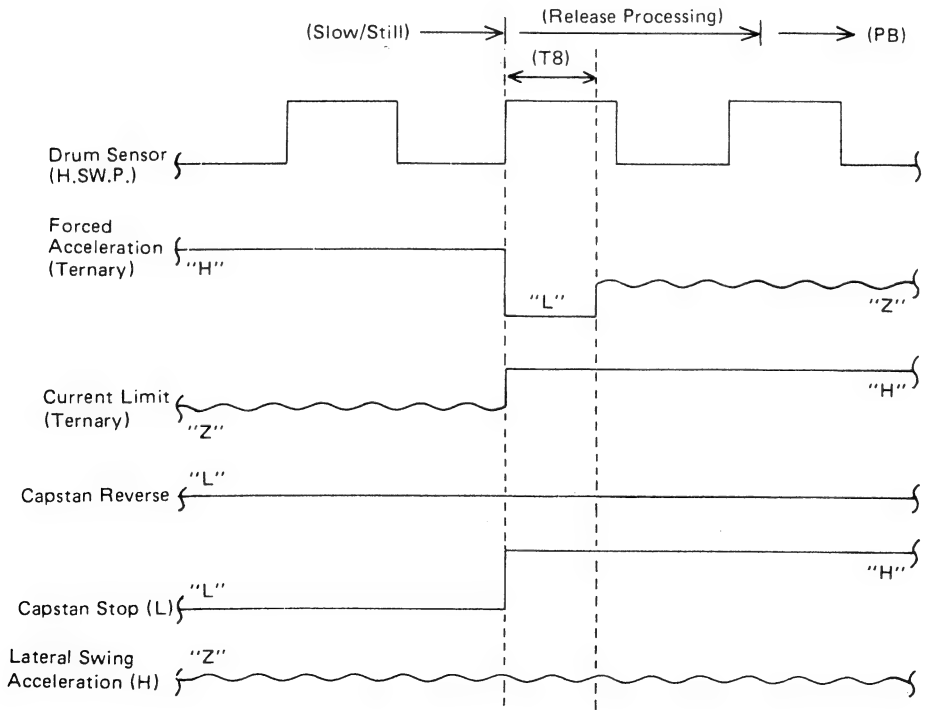


Figure 4-3.

Symbol		Item	Preset Value		
			SP	LP	
Frame Advancing	T0	Start M/M	13.8 ms	—	
	T1	Forced acceleration M/M	16.6 ms	—	
	T2	Lateral swing acceleration start time	18.7 ms	—	
	T3	Lateral swing acceleration M/M	45.8 ms	—	
	T4	Speed reduction M/M	12.0 ms	—	
	T5	Brake M/M	13.6 ms	—	
	T6	———	—	—	
	T7	———	—	—	
Release	T8	Forced acceleration release	23.0 ms	—	
	T9	———	—	—	

Note: Head 2 is special for SP; therefore, Slow/Still M/M, etc. of LP is under study.

Table 4-1.

Slow/Still Frame Advance Timing Chart (4-head system)

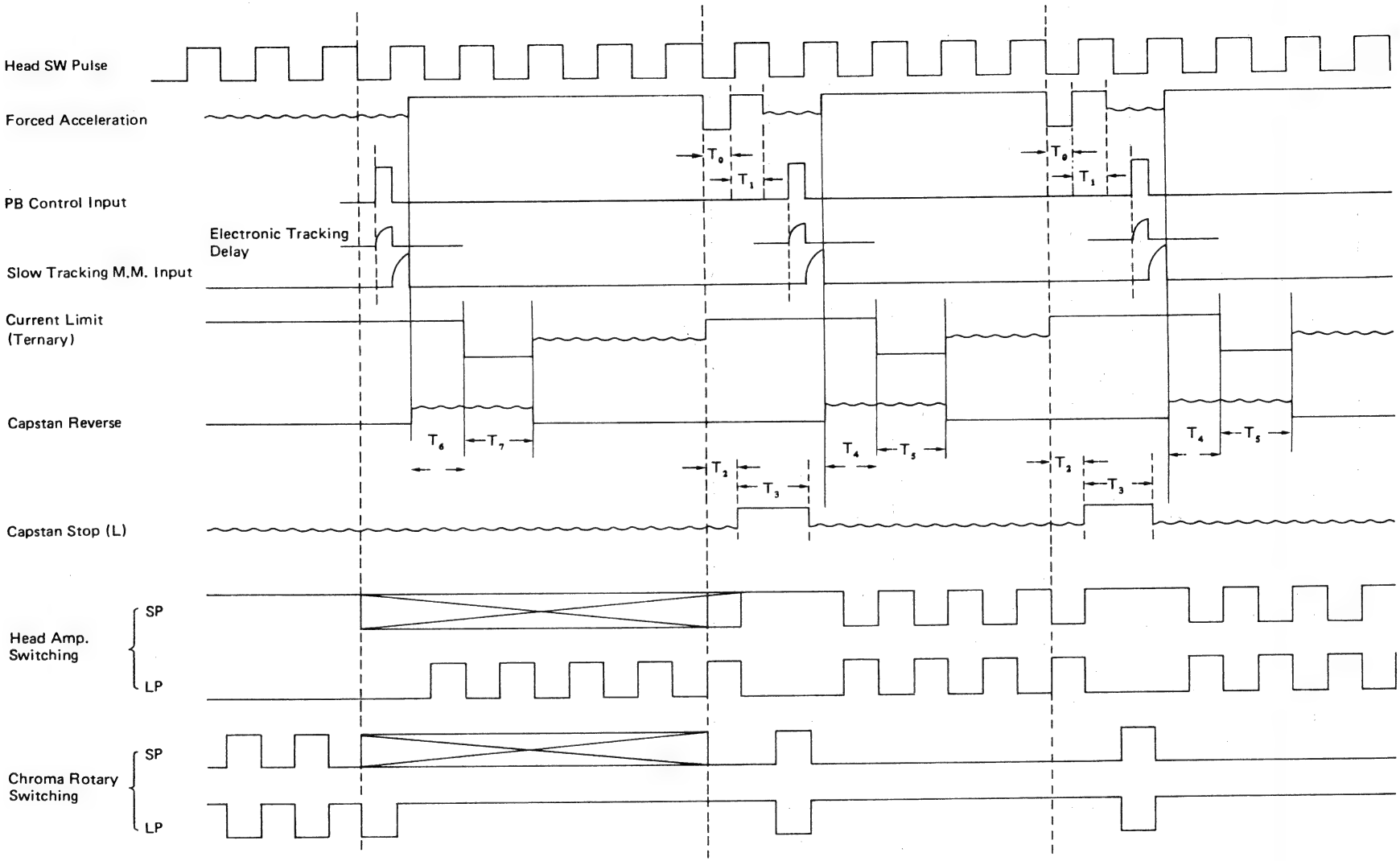


Figure 4-4.

Shift to PB mode when the SP Slow/Still mode is cleared (4-head system)

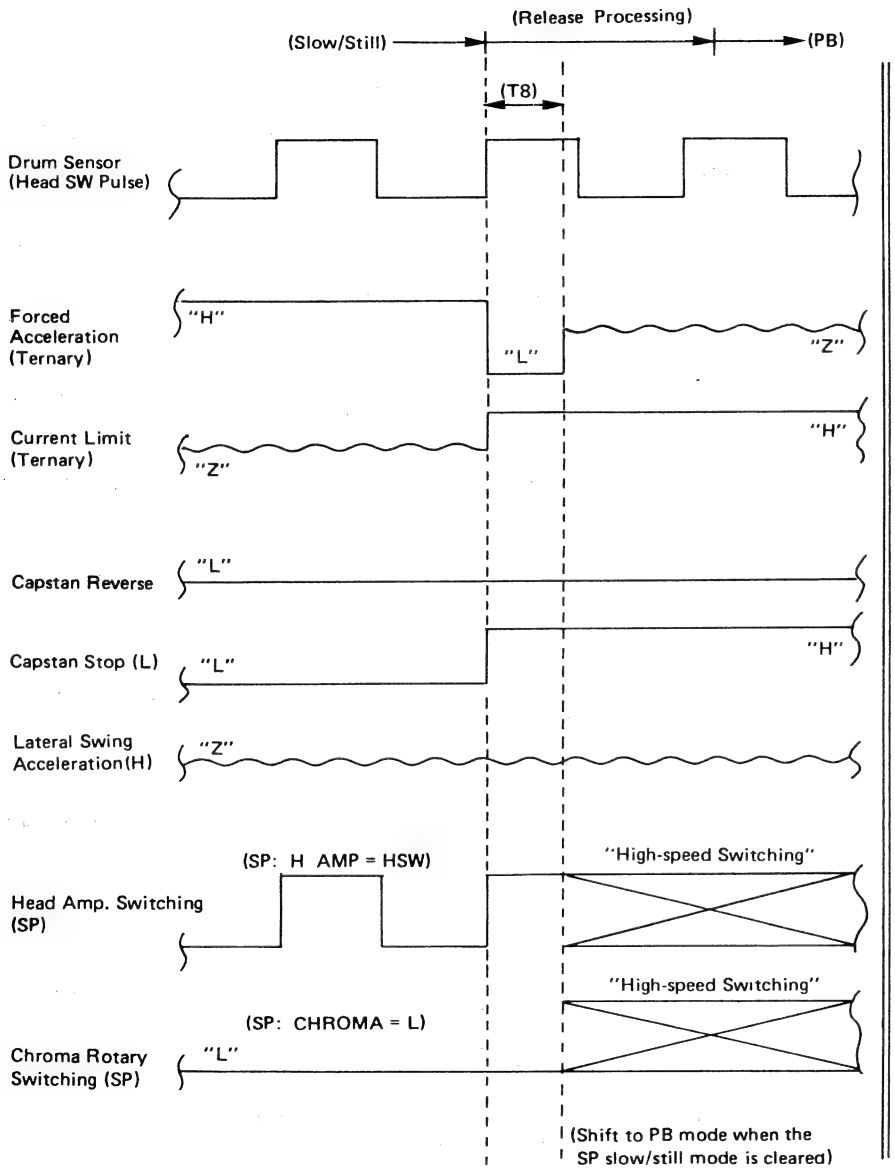


Figure 4-5.

Shift to PB mode when the LP Slow/Still mode is cleared (4-head system)

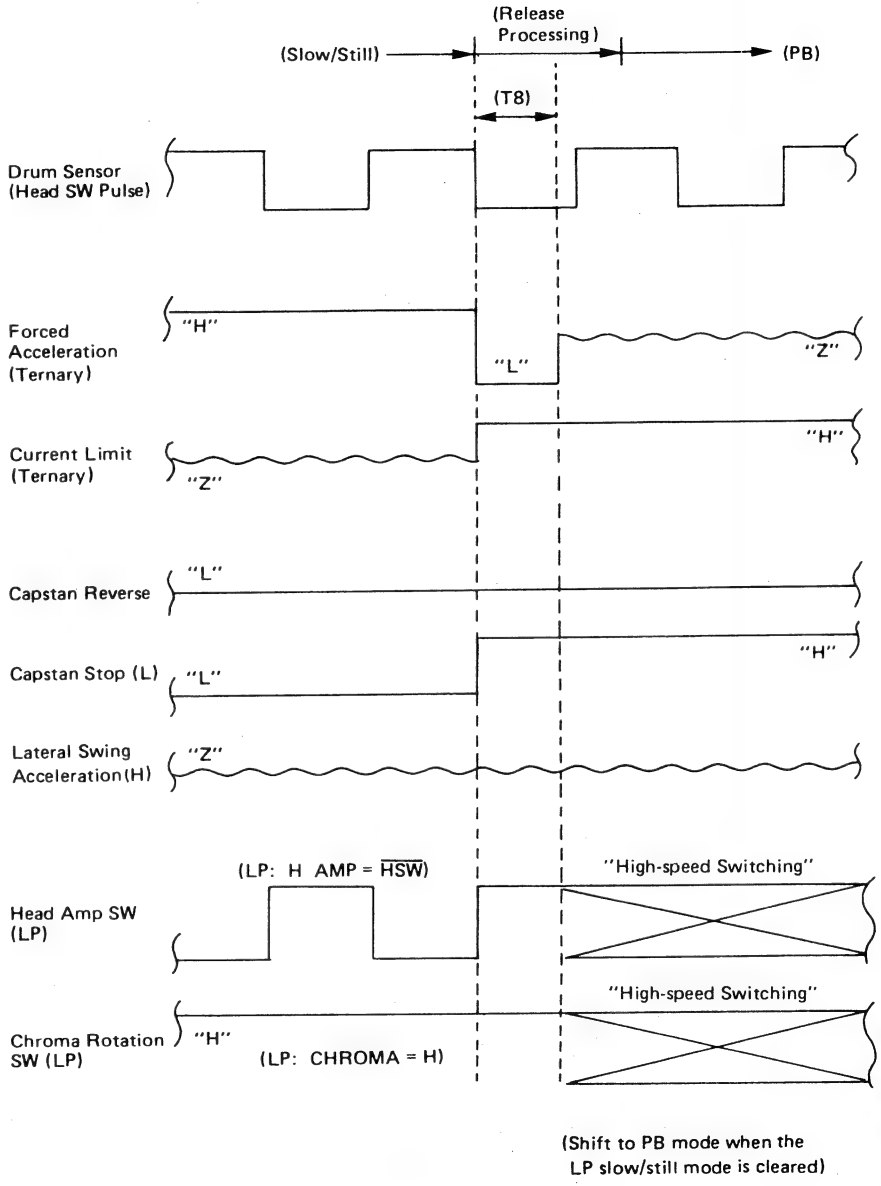


Figure 4-6.

Shift to REC/STOP mode when the SP Slow/Still mode is cleared (4-head system)

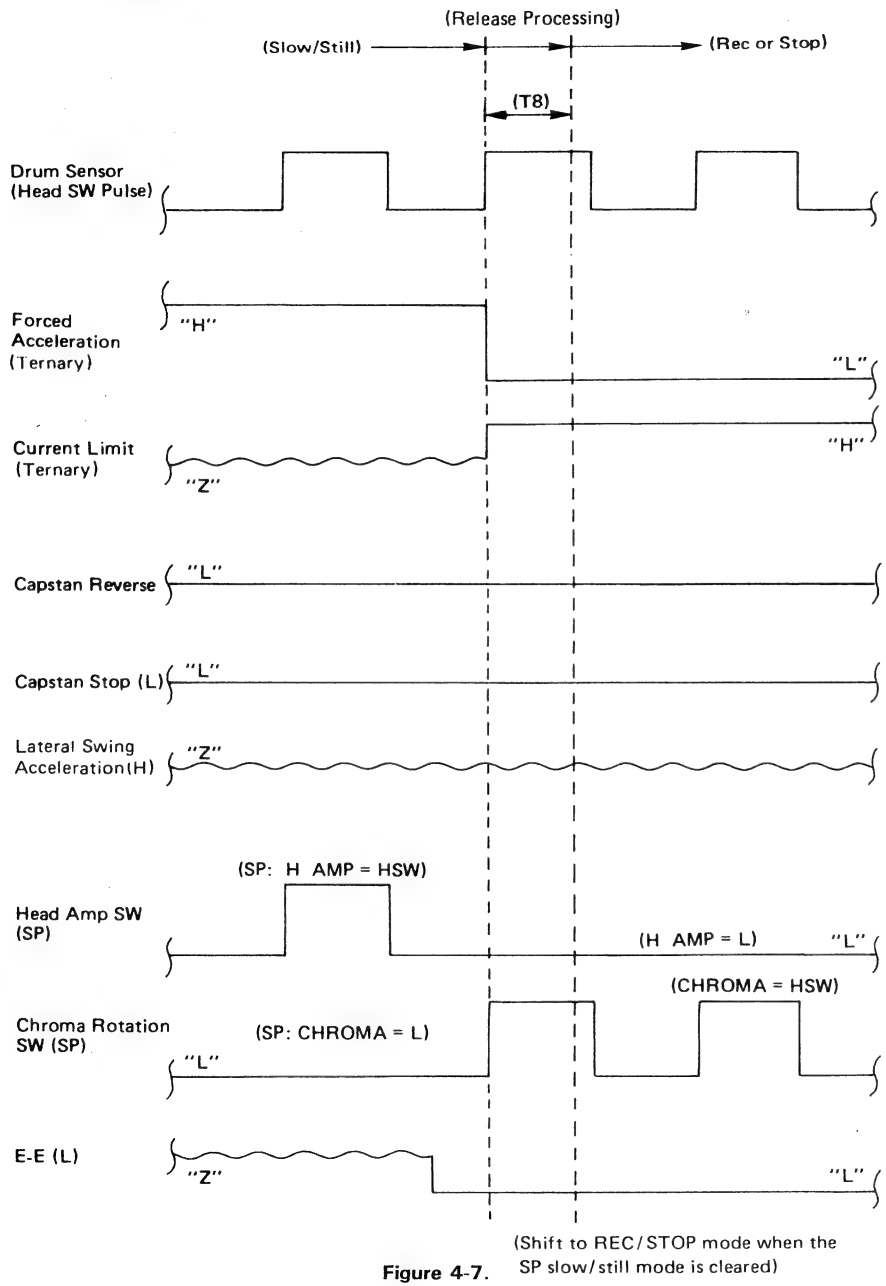


Figure 4-7.

Shift to REC/STOP mode when the SP Slow/Still mode is cleared (4-head system)

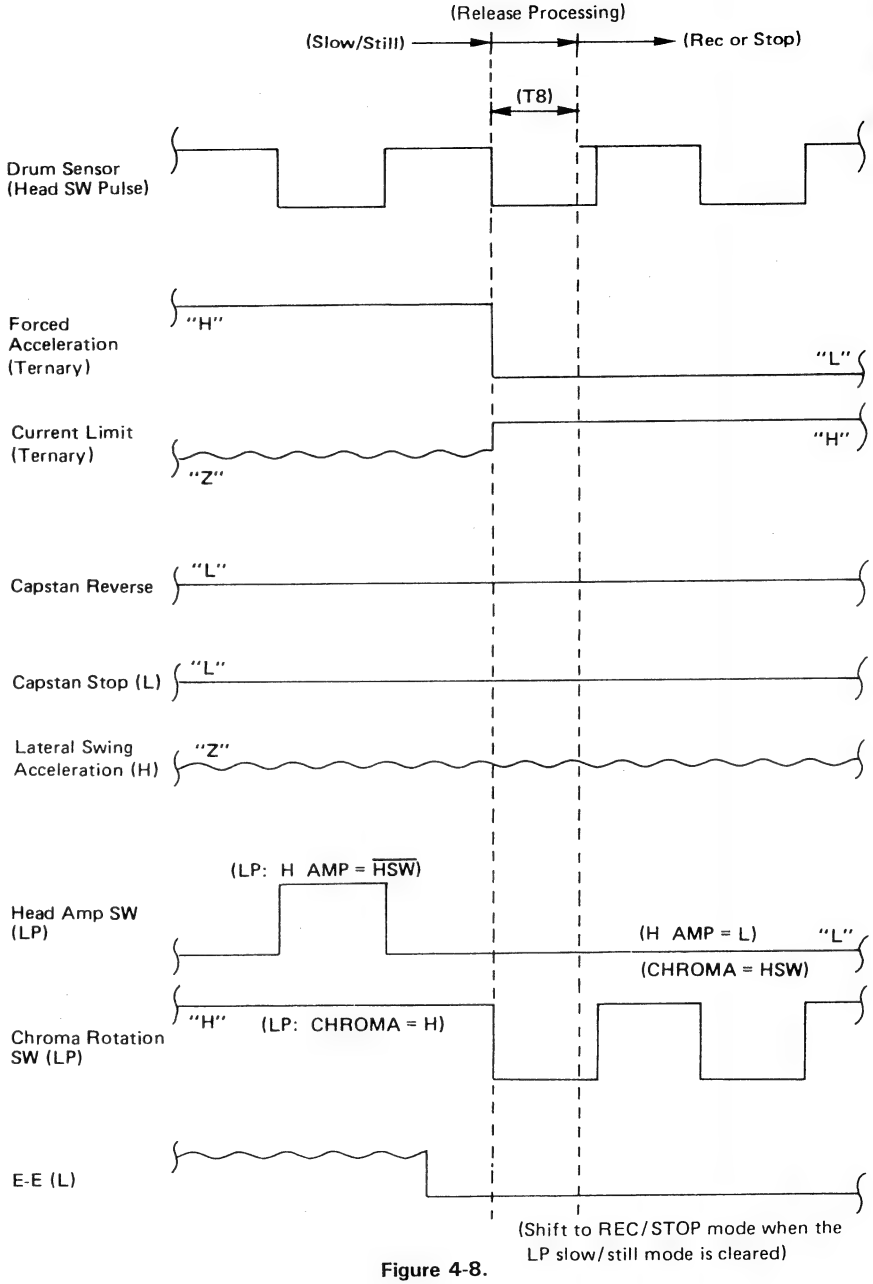


Figure 4-8.

Symbol		Item	Preset Value		
			SP	LP	
Frame Advancing	T0	Start M/M	14.08 ms	9.73 ms	
	T1	Forced acceleration M/M	18.94 ms	11.01 ms	
	T2	Lateral swing acceleration start time	23.04 ms	19.46 ms	
	T3	Lateral swing acceleration M/M	23.81 ms	33.28 ms	
	T4	Speed reduction M/M	11.78 ms	5.12 ms	
	T5	Brake M/M	12.29 ms	3.58 ms	
	T6	Speed reduction M/M (At Still On)	11.78 ms	7.94 ms	
	T7	Brake M/M (At Still On)	12.29 ms	3.58 ms	
Release	T8	Forced acceleration release	23.04 ms	9.22 ms	
	T9	———	——	—	

Note: Head 2 is special for SP; therefore, Slow/Still M/M, etc. of LP is under study.

Table 4-2.

5. TIMER CIRCUIT

5-1. The RH-IX0581GEZZ is a timer microcomputer LSI featuring the channel selection function by a voltage synthesizer tuner.
(VC-A103, A116, A125, A118, A508, A615, T620 Series and VC-A215H)

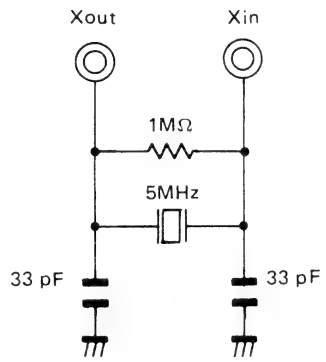
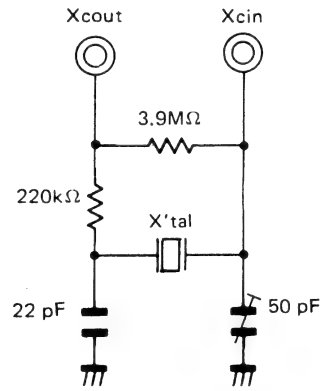
- **Terminal Allocation (RH-iX0581GEZZ)**

Terminal Name	No.	Name		Name	No.	Terminal Name
G11	64	P40		Vcc	1	+5V
G10	63	P41		P65	2	AUDIO OUTPUT CTL
G9	62	P42		P64	3	E^2 PROM CS
G8	61	P43		P63	4	E^2 PROM CLK
G7	60	P44		P62	5	E^2 PROM S0/S1/OSD S0
G6	59	P45		P61	6	PWM OUTPUT
G5	58	P46		P60	7	AFT MUTE
G4	57	P47		P27	8	B0
G3	56	P00		P26	9	B1
G2	55	P01		P25	10	OSD MUTE/BLUE BACK
G1	54	P02		P24	11	OSD CLK
S13	53	P03		P23	12	OSD CS-(L)
S12	52	P04		P22	13	CTL FREQ. DIV. IC RESET
S11	51	P05		P21	14	SECAM OSD PROHIBIT INPUT
S10	50	P06		P20	15	NORMAL (L)
S9	49	P07	RH-iX0581GEZZ	Srdy	16	SYSCON READY-(L)
S4	48	P10		CLK	17	SYSCON/TIMER CLK
S5	47	P11		Sout	18	TIMER SERIAL DATA
S3	46	P12		Sin	19	SYSCON SERIAL DATA
S7	45	P13		P33	20	CTL PULSE (1/25)
S6	44	P14		P32	21	INTERNAL COUNTER CLK INPUT
S2	43	P15		P31	22	VIDEO TUNER (H)
S1	42	P16		P30	23	AUDIO TUNER (H)
S8	41	P17		INT1	24	A/C PULSE
NC	40	P50		INT2	25	R/C PULSE INPUT
PAY (H)	39	P51		CNV_{ss}	26	GND
−30V	38	Vp		RESET	27	RESET -(L)
KEY INPUT 1	37	P54		Xin	28	CLOCK INPUT
KEY INPUT 2	36	P55		Xout	29	CLOCK OUTPUT
KEY INPUT 3	35	P56		XCin	30	CLOCK INPUT FOR TIMER
KEY INPUT 4	34	P57		XCout	31	CLOCK OUTPUT FOR TIMER
X'TAL ADJ.	33	ϕ		V_{ss}	32	GND

Figure 5-1.

5-2. TERMINAL DESCRIPTION (RH-iX0455GEZZ: Voltage synthesizer tuner)

Pin No.	Name	Description	I/O (Type)
1	Vcc	At 5V to be connected.	
2	AUDIO OUTPUT CTL	Control signal to switch the audio output between (L+R), L, R and NORMAL.	O (C-MOS)
3	E^2PROM CS	Used for serial transfer between Timer and E^2PROM. Note that pin No. 5 (E^2PROM SI/SO/OSD SO) is commonly used as the OSD Control serial port.	O (C-MOS)
4	E^2PROM CLK		O (C-MOS)
5	OSD SO/E^2PROM SI/SO		I/O (C-MOS)
6	PWM OUTPUT	Tuning voltage PWM output. 14-bit resolution.	O (C-MOS)
7	AFT MUTE	Output when the volsyn is in preset mode or when tuning is being done.	O (C-MOS)
8	B0	Band switching output for tuning	O (N-CH)
9	B1		O (N-CH)
10	OSD MUTE/ BLUE BACK	OSD control serial terminal.	O (N-CH) O (N-CH)
11	OSD CLK		O (N-CH)
12	OSD CS-(L)		O (N-CH)
13	CTL FREQ. DIV. IC RESET	Control signal to reset the CTL frequency dividing IC.	O (N-CH)
14	SECAM OSD PROHIBIT INPUT	Control signal to prohibit the superimpose function while receiving SECAM signal.	I
15	NORMAL (L)	Terminal commonly used for forced normal (L) output and LR display mute (L) input. (A mute signal is supplied via the N-CH open drain circuit. On Hi-Fi models.)	O (N-CH)
16	SYSCON READY-(L)	Control signal for serial transfer between timer and system controller.	I
17	SYSCON/TIMER CLK		O (N-CH)
18	TIMER SERIAL DATA		O (N-CH)
19	SYSCON SERIAL DATA		I
20	CTL PULSE (1/25)	1-second count source input for the real time counter.	I
21	INTERNAL COUNTER CLK INPUT	Clock count input for the timer. Connected to Pin No. 31. Shortest pattern possible to be taken for connection.	I
22	VIDEO TUNER (H)	Input switching control terminal.	O (N-CH)
23	AUDIO TUNER (H)		O (N-CH)

Pin No.	Name	Description	I/O (Type)
24	A/C PULSE	A/C-shaped signal input for power failure detection. Power failure is identitied if there is no change in A/C pulse for 35 msec. External interrupt at the rising edge.	I
25	R/C PULSE INPUT	Rising edge of R/C pulse is detected. External interrupt at the rising edge to measure the interval between two rising edges of R/C pulse.	I
26	CNVss	Connected to GND (0V).	
27	RESET-(L)	All Clear is made when a voltage lower than 0.6V has been put in for 2 μsec or more after the supply voltage reached the microcomputer's operating voltage (5V ± 10%).	I
28 29	CLOCK INPUT CLOCK OUTPUT	System clock generating circuit built-in. System clock is obtained by adding a ceramic resonance circuit as shown below.  Figure 5-2.	I O
30 31	CLOCK INPUT FOR TIMER CLOCK OUTPUT FOR TIMER	Timer count clock generating circuit built-in. Timer count clock is obtained by adding a crystal resonance circuit as shown below.  Figure 5-3.	I O
32	Vss	Connected to GND (0V).	

Pin No.	Name	Description	I/O (Type)
33	X'tal ADJ.	Crystal adjustment output. Adjustment is made when the microcomputer is reset. Half the crystal output (32.768 kHz) is given out with jumper provided.	O
34 35 36 37	KEY INPUT 4 KEY INPUT 3 KEY INPUT 2 KEY INPUT 1	4 x 13 matrix is formed by Pin Nos. 41 thru 53 (S1 thru S2). Jumper input or key input is made.	I I
38	Vp	– 30V to be connected	

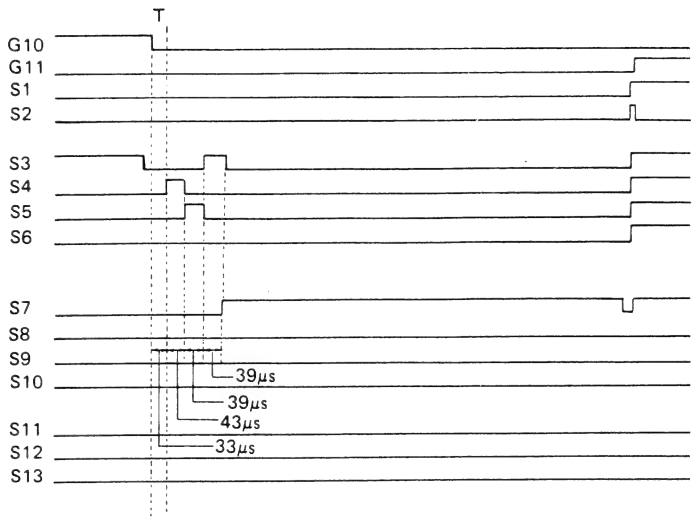


Figure 5-4.

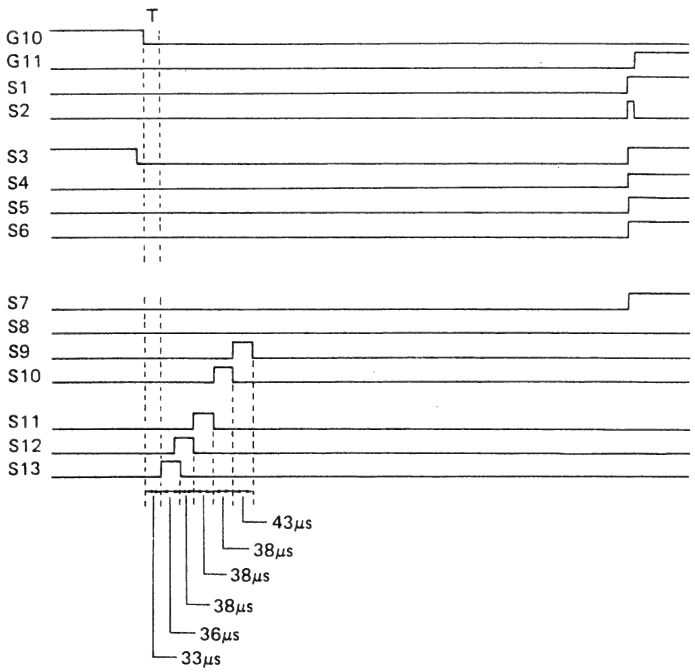


Figure 5-5.

Pin No.	Name	Description	I/O (Type)
39	PAY (H)	Output at "H" while the PAY position is selected.	O (P-CH)
40	NC		
41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64	S8 S1 S2 S6 S7 S3 S5 S4 S9 S10 S11 S12 S13 G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11	Output terminals for fluorescent display tube drive segment signal and key scan strobe signal. (Segment signal) Segment signal output is timed with digit signal output at Pins 54 thru 64.	O (P-CH) High withstand voltage

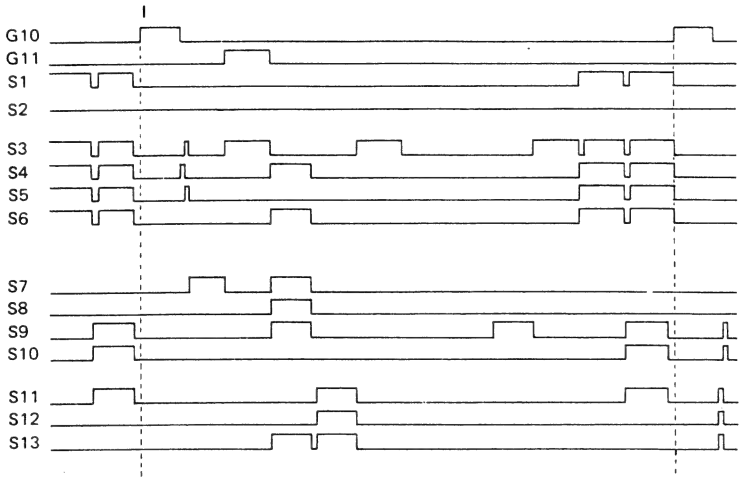
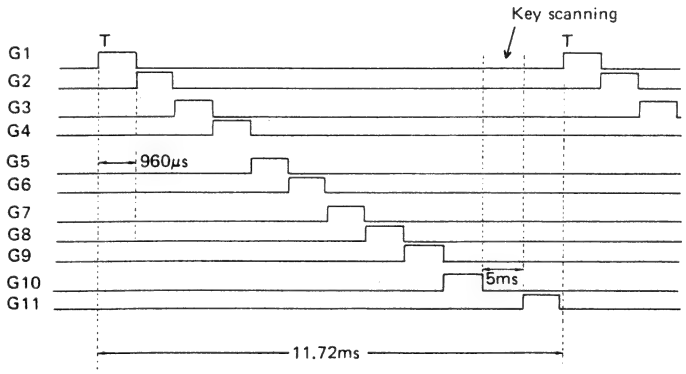
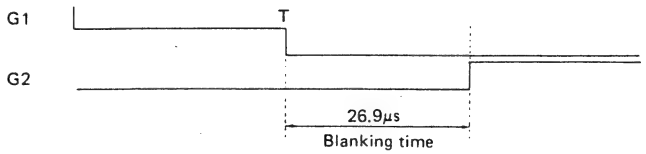


Figure 5-6.

	Output terminals for digit signals to drive the fluorescent display tube.	O (P-CH) High withstand voltage





$$\text{Display duty} = \frac{960\mu s}{11.72ms} = \frac{1}{12.21}$$

Figure 5-7.

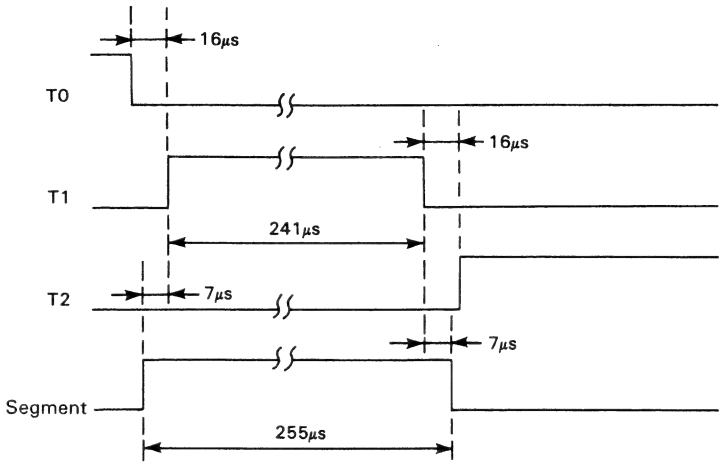
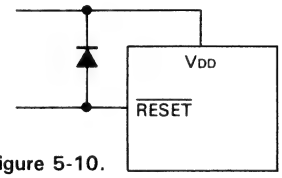
5-3. The RH-IX0580GEZZ and RH-IX0584GEZZ are a timer microcomputer LSI featuring the channel selection function by a frequency synthesizer tuner.
(VC-A615G(BK), GM(BK), YM(BK), VC-A215S(BK), VC-A103GV(BK), VC-A106GVM(BK))

- **Terminal Allocation (RH-iX0580GEZZ, RH-iX0584GEZZ)**

Terminal Name	No.	Name		Name	No.	Terminal Name
+5V	64	V_{DD}		S3	1	S6
S7	63	S4		S2	2	S2
S3	62	S5		S1	3	S1
S5	61	S6		S0	4	S8
S4	60	S7		INT4	5	AC PULSE
S9	59	S8		$\overline{SCK}$	6	SYSCON/TIMER-CLK
S10	58	S9		SO	7	TIMER SERIAL DATA
−4V	57	V_{PRE}		SI	8	SYSCON SERIAL DATA
−30V	56	V_{LOAD}		INT0	9	R/C PULSE
MODE OSD (H)	55			INT1	10	SYSCON READY (L)
NC	54			INT2	11	CTL PULSE (1/25)
S11	53	S12		P13	12	SECAM OSD PROHIBIT INPUT
S12	52	S13		P20	13	CTL FREQ. DIV. IC RESET
S13	51	S14		P21	14	VCR (L)
G11	50	T10	RH-iX0580GEZZ RH-iX0584GEZZ	P22	15	TUNER (H)
G10	49	T9		BUZ	16	PAY (H)/TUNER-PCON
G9	48	T8		P30	17	A-AUX (H)
G8	47	T7		P31	18	MIX (H)
G7	46	T6		P32	19	A-AUX2 (H)
G6	45	T5		P33	20	21 PIN CTL (H)
G5	44	T4		P60	21	AUDIO-OUTPUT-CTL
G4	43	T3		P61	22	NORMAL (L)
G3	42	T2		P62	23	SCL
G2	41	T1		P63	24	SDA
G1	40	T0		P40	25	KEY 1
$\overline{RESET}$	39	$\overline{RESET}$		P41	26	KEY 2
OSD CLK	38	P53		P42	27	KEY 3
OSD DATA	37	P52		P43	28	KEY 4
OSD CS (L)	36	P51		PPO	29	NC
OSD MUTE	35	P50		X1	30	4MHZ
32.768 kHz	34	XT2		X2	31	4MHz
32.768 kHz	33	XT1		Vss	32	GND

Figure 5-8.

5-4. TERMINAL DESCRIPTION (RH-iX0580GEZZ, RH-iX0584GEZZ)

Pin No.	Name	Description	I/O
1 2 3 4 51 52 53 58 59 60 61 62 63	S6 S2 S1 S8 S13 S12 S11 S10 S9 S4 S5 S3 S7	Output terminals for segment signals to drive the fluorescent display tube.  Figure 5-9.	O
5	AC PULSE	Used to detect service interruption. It detects service interruption when there is no change in leading or trailing edge for more than 35 ms, and the microcomputer goes into service interruption mode. DUTY is 25% ~ 75%. V_{DD} and this terminal are connected with diode.  Figure 5-10.	I
6	SYSCON/TIMER CLK	Used for serial transferring with the system controller. Connected to the CLK terminal of system controller. N-ch open	O
7	TIMER SERIAL DATA	Used for serial transferring with the system controller. Connected to the timer serial data terminal of system controller. N-ch open	O
8	SYSCON SERIAL DATA	Used for serial transferring with the system controller. Connected to the syscon serial data terminal of system controller. Schmidt trigger input with hysteresis characteristic.	I
9	R/C PULSE	Terminals to input pulses from optical remote control light receiving position. Receive criterion of leading interval (T) of pulses is as follows: T < 0.4 ms ..... Pulse invalid 0.4 ms ≦ T < 1.6 ms ..... Logic "0" 1.6 ms ≦ T < 3.2 ms ..... Logic "1" 3.2 ms ≦ T ..... Pulse end	I
10	SYSCON READY (L)	Used for serial transferring with the system controller. Connected to the READY-L terminal of system controller. Schmidt trigger input with hysteresis characteristic.	I

<table>
<tr><th>Pin No.</th><th>Name</th><th>Description</th><th>I/O</th></tr>
<tr><td>11</td><td>CTL PULSE (1/25)</td><td>Signal to control real time counter.
When leading or trailing edge input of CTL pulse is performed with PCON bit = ''1'' and cassette-in bit = ''1'', it makes internal counter UP for 0.5 sec with counter inversion bit = ''0'' and DOWN for 0.5 sec with counter inversion bit = ''1''.
Counter inversion bit — Syscon serial data (S34) to show Normal rotation/Inversion of the drum.</td><td>I</td></tr>
<tr><td>12</td><td>SECAM OSD PROHIBIT INPUT</td><td>In case of SECAM input terminal = ''H'', SECAM bit is ''1''; in case of SECAM input terminal = ''L'', SECAM bit is ''0''.</td><td>I</td></tr>
<tr><td>13</td><td>CTL FREQ. DIV. IC RESET</td><td>Signal to reset 1/25 dividing IC.
Reset terminal turns ''H'' for 1 ms when zero reset of counter value or dividing IC is performed.</td><td>O</td></tr>
<tr><td>14</td><td>VCR (L)</td><td>Syscon data VCR mode bit (S_{26}) = ''0'' → VCR(L) = ''H''
Syscon data VCR mode bit (S_{26}) = ''1'' → VCR(L) = ''L''</td><td>O</td></tr>
<tr><td>15</td><td>TUNER (H)</td><td>Inpunt switching control output terminal
<table>
<tr><th>TUNER mode</th><th>SIMUL mode</th><th>AUX1 mode</th><th>AUX2 mode</th></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td></tr>
</table>
Table 5-1.</td><td>O</td></tr>
<tr><td>16</td><td>PAY (H)/
TUNER-PCON</td><td>It corresponds to PAY when PAY jumper is present, and becomes tuner-PCON output function when PAY jumper is not present.
PAY(H) — Displaying ''+3'' when selecting CH3 with AUS jumper present.
Displaying ''+4'' when selecting CH4 with AUS jumper not present.
Tuner PCON — Signal to control the tuner power supply for receiving VHS code even if in ''POWER OFF'' state during timer stund-by.
Tuner PCON = ''H'' when detecting VPS timer value and performing VPS timer picture recording.</td><td>O</td></tr>
<tr><td>17
19</td><td>A-AUX (H)
A-AUX2 (H)</td><td>Input switching control output terminal.
<table>
<tr><th></th><th>TUNER mode</th><th>SIMUL mode</th><th>AUX1 mode</th><th>AUX2 mode</th></tr>
<tr><td>A-AUX (H)</td><td>L</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>A-AUX2 (H)</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
</table>
Table 5-2.</td><td>O</td></tr>
<tr><td>18</td><td>MIX (H)</td><td>When EE bit = ''1'' or EE bit = ''0'', and SO byte = insert, this terminal is inverted regarding MIX KEY as valid.
When EE bit = ''1'' and SO byte = insert, this terminal turns ''L'' regarding MIX KEY as invalid.</td><td>O</td></tr>
<tr><td>20</td><td>21 PIN CTL (H)</td><td>Conditions for terminal = ''H''
1) EE bit = ''0''
2) During programmed OSD display
3) TSE bit = ''1''
In conditions other than the above ones, this terminal turns ''L''.</td><td>O</td></tr>
</table>

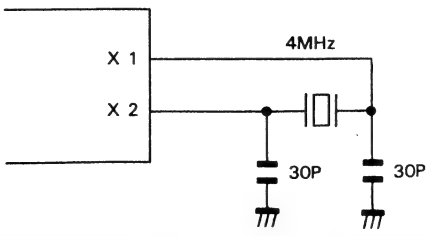
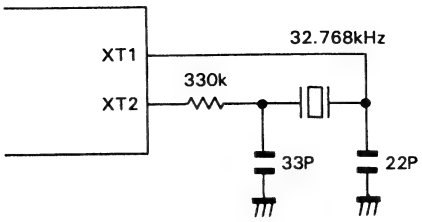
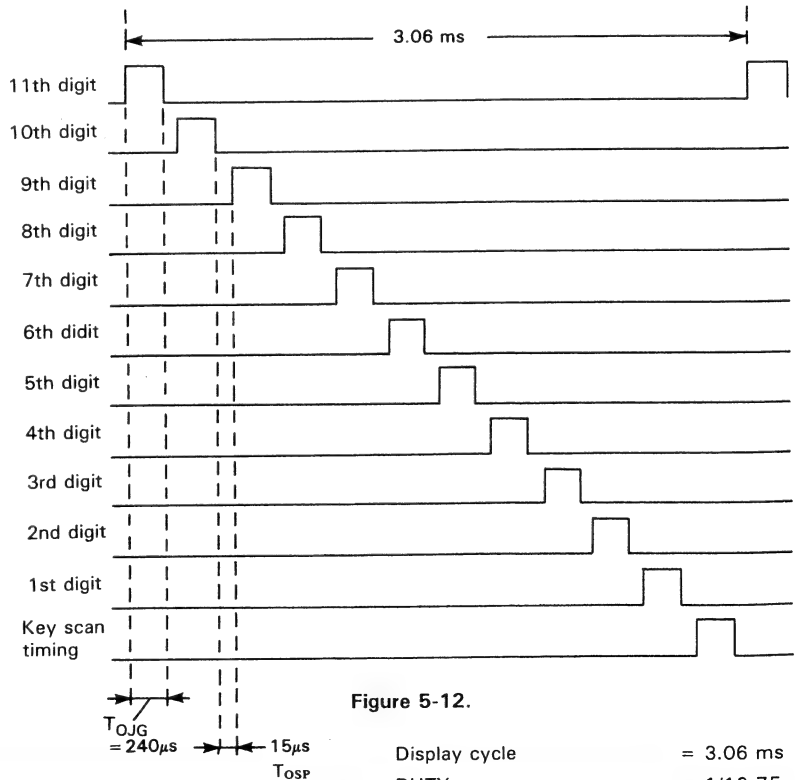
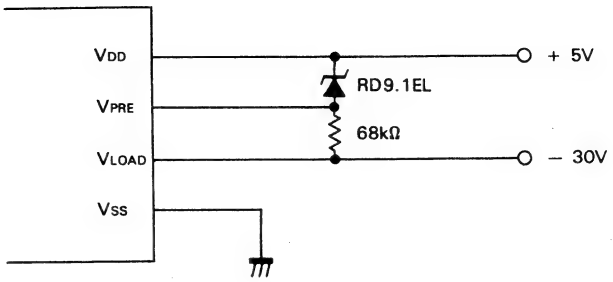
<table>
<tr><th>Pin No.</th><th>Name</th><th>Description</th><th>I/O</th></tr>
<tr><td>21</td><td>AUDIO-OUTPUT-CTL</td><td>Audio output switching control signal
<table>
<tr><th>MODE</th><th>AUDIO-OUTPUT-CTL</th></tr>
<tr><td>Stereo (Main + Sub)</td><td>L</td></tr>
<tr><td>Left (Main)</td><td>High impedance</td></tr>
<tr><td>Right (Sub)</td><td>H</td></tr>
<tr><td>Forced NOR</td><td>L</td></tr>
</table>
Table 5-3.
It is in stereo mode when the microcomputer is reset.</td><td>O</td></tr>
<tr><td>22</td><td>NORMAL (L)</td><td>''L.R.HiFi'' display is put out when this terminal is ''L''.
<table>
<tr><th></th><th></th><th>Normal L terminal</th></tr>
<tr><td>L+R</td><td>H-L, R ON
L-L, R OFF</td><td>Input</td></tr>
<tr><td>L</td><td>H-L ON
L-L OFF</td><td>Input</td></tr>
<tr><td>R</td><td>H-R ON
L-R OFF</td><td>Input</td></tr>
<tr><td>NORMAL</td><td>L output</td><td>Output</td></tr>
</table>
Table 5-4.</td><td>I/O</td></tr>
<tr><td>23</td><td>SCL</td><td>Used for serial communication with the VPS decoder. By converting L to H at the ninth bit (ACK), it transfers ''H'' or ''L'' from the receiving side to sending side.
''H'' is selected when the I^2C bus is not used.</td><td>I/O</td></tr>
<tr><td>24</td><td>SDA</td><td>Terminal for I^2C bus control.
''H'' is selected when the I^2C bus is not used.
With SCL being ''H'', when the terminal experiences ''H'' → ''L'' conversion, data transferring starts; when the terminal experience ''L'' → ''H'' conversion, data transferring ends.</td><td>I/O</td></tr>
<tr><td>25
26
27
28</td><td>KEY 1
KEY 2
KEY 3
KEY 4</td><td>Input terminals for jumper and key, which compose 4X matris.</td><td>I</td></tr>
<tr><td>29</td><td>NC</td><td>Open</td><td></td></tr>
<tr><td>30
31</td><td>MAIN SYSTEM
CLOCK</td><td>Main system clock is obtained.


Figure 5-11.</td><td>I
O</td></tr>
</table>

Pin No.	Name	Description	I/O
32	GND	GND (0V)	
33 34	SUB SYSTEM CLOCK	Sub system clock is obtained.  **Figure 5-12.**	I O
35	OSD MUTE	Outputting "H" when controlling OSD IC. Displaying blue mute and emblem for OSD IC. OSD mute terminal turns "H" when displaying programmed content.	O
36	OSD CS (L)	Used for serial transferring with OSD. Connected to $\overline{CS}$ terminal of OSD IC. Being "L" only when accessing OSD IC.	O
37	OSD DATA	Used for serial transferring with OSD. Connected to the SO terminal of OSD IC.	O
38	OSD CLK	Used for serial transferring with OSD. Connected to serial CLK terminal of OSD IC.	O
39	$\overline{RESET}$	The microcomputer is reset when $\overline{RESET}$ = "L".	
40 41 42 43 44 45 46 47 48 49 50	G11 G10 G9 G8 G7 G6 G5 G4 G3 G2 G1	Output terminals for digit signals to drive the fluorescent display tube. P-ch open. Pull-down resistance built-in.  **Figure 5-12.** Display cycle = 3.06 ms DUTY = 1/12.75 Digit signal cutting amplitude = 1/16	O

Pin No.	Name	Description	I/O
54	NC	Open	
55	MODE OSD (H)	This terminal turns "H" during OSD output in OSD mode.	O
56 57	−30V −4V	−30V −4V  Figure 5-13.	
64	+5V	V_{DD}(+5V)	

6. AUTOMATIC VOLTAGE SYNTHESIZER CIRCUIT

6-1. Terminal Description of Automatic Voltage Synthesizer IC RH-iX0600GEZZ (VC-A615G(BK), GM(BK), YM(BK), VC-A215S(BK), VC-A103GV(BK), VC-A106GVM(BK))

- **Terminal Allocation (RH-iX0600GEZZ)**

Terminal Name	No.	Name		Name	No.	Terminal Name
AT 5V	48	AD0		POC3	1	NC
AFT-S CURVE IN	47	P1C1		POC2	2	NC
NC	46	P1C2		POC1	3	NC
NC	45	P1C3		POC0	4	NC
T.A DATA	44	P0A0		POD3	5	JUMPER IN
T.A CLOCK	43	P0A1		POD2	6	VHF/UHF SELECT SW
CS	42	P0A2		POD1	7	KEY-1
CLOCK	41	P0A3		POD0	8	KEY-2
DATA I/O	40	P0B0		P1D3	9	NC
B0	39	D0B1		P1D2	10	NC
B1	38	P0B2		P1D1	11	NC
$\overline{\text{SYNC DET}}$	37	P0B3		P1D0	12	NC
$\overline{\text{V SYNC}}$	36	$\overline{\text{VSYNC}}$		VDD	13	AT 5V
$\overline{\text{H SYNC}}$	35	$\overline{\text{HSYNC}}$	RH-iX0600GEZZ	CE	14	AT 5V
NC	34	BLANK		INT	15	NC (GND)
NC	33	B		GND	16	GND
NC	32	G		P1A3	17	NC
NC	31	R		P1A2	18	NC
VT PULSE	30	PWM rmp		P1A1	19	NC
AFT MUTE	29	PWM0		P1A0	20	NC
V-MUTE	28	PWM1		XO	21	8-MHz
NC	27	PWM2		XI	22	8-MHz
NC (AT 5V)	26	P1B0		P1B3	23	NC
NC (AT 5V)	25	P1B1		P1B2	24	NC

Figure 6-1.

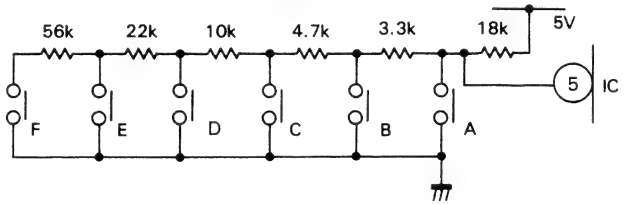
<table>
<tr><th>Pin No.</th><th>Name</th><th>Terminal</th><th>Description</th><th>I/O</th></tr>
<tr><td>1
2
3
4</td><td>NC</td><td>POC3
POC2
POC1
POC0</td><td></td><td></td></tr>
<tr><td>5</td><td>JUMPER INPUT</td><td>P0D3</td><td>
<table>
<tr><th>Jump</th><th>Analog data</th><th colspan="3">Digital data</th><th>Content</th></tr>
<tr><td>A</td><td>0 [V]</td><td>0</td><td>0</td><td>0</td><td>AV1 system HYPER not corresponding 60 POSI</td></tr>
<tr><td>B</td><td>0.77</td><td>0</td><td>0</td><td>1</td><td>AV1 system HYPER not corresponding 99 POSI</td></tr>
<tr><td>C</td><td>1.54</td><td>0</td><td>1</td><td>0</td><td>AV1 system HYPER corresponding 60 POSI</td></tr>
<tr><td>D</td><td>2.50</td><td>0</td><td>1</td><td>1</td><td>AV1 system HYPER corresponding 99 POSI</td></tr>
<tr><td>E</td><td>3.45</td><td>1</td><td>0</td><td>0</td><td>AV2 system HYPER not corresponding 99 POSI</td></tr>
<tr><td>F</td><td>4.21</td><td>1</td><td>0</td><td>1</td><td>AV2 system HYPER not corresponding 60 POSI</td></tr>
<tr><td></td><td>5.0</td><td>1</td><td>1</td><td>0</td><td>AV2 system HYPER corresponding 99 POSI</td></tr>
</table>
60/99 bit — 60 POSI = 0, 99 POIS = 1
Hyper bit — Not corresponding = 0, Corresponding = 1
AV2 bit — AV1 system = 0, AV2 system = 1
Table 6-1.


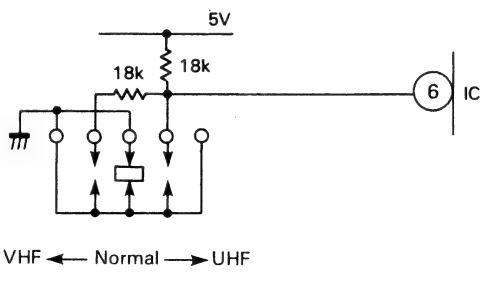
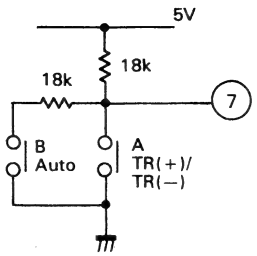
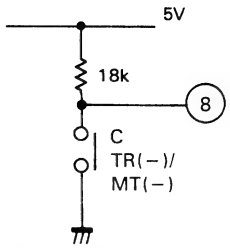
Figure 6-2.
Terminal to perform A/D conversion of pin ⑤ input voltage (analog data) and convert it into digital data.
By identifying this digital data, the selection specified above is performed.
VC-A615G ..... D,
VC-A615GM, YM
VC-A103GV ..... A
VC-A215S
VC-A106GVM
</td><td>I</td></tr>
<tr><td>6</td><td>VHF/UHF SELECT SW</td><td>P0D2</td><td>


Figure 6-3.
Tuning (UHF, VHF) and Normal modes are identified with pin ⑥ input voltage.
</td><td>I</td></tr>
</table>

Pin No.	Name	Terminal	Description	I/O
7 8	KEY-1 KEY-2	P0D1 P0D0	 Figure 6-4. KEY-1  Figure 6-5. KEY-2 With three pieces of SW, this terminal identifies MT (+) and (−) and makes VT up and down in Tuning mode; it identifies TR (+) and (−) and changes tracking in Normal mode.	I
9 10 11 12	NC	P1D3 P1D2 P1D1 P1D0		
13	AT 5V	V_{DD}	Power supply input. 5±0.5V.	
14	AT 5V	CE	Selector signal input terminal. It is made High (5V) in normal operation.	I
15	NC (GND)	INT		
16	GND	GND	GND	
17 18 19 20	NC	P1A3 P1A2 P1A1 P1A0		
21 22	8MHz 8MHz	XO XI	Terminal for system clock. Oscillator of 8 MHz is connected to this terminal.	
23 24	NC	P1B3 P1B2		
25	Bilingual IN (L)	P1B1	In case of "L", bilingual display is lit. Connected to AT 5V because of no display.	I
26	Stereo IN (L)	P1B0	In case of "L", stereo display is lit. Connected to AT 5V because of no display.	I
27	NC	PWM2		
28	V-MUTE	PWM1	Conditions for Video Mute. • When EE bit = "1" and there is no video signal, V-Mute = "H" is made. • When EE bit = "0", V-Mute = "L" is made. • When EE bit is changed from "1" to "0", V-Mute = "L" is continued for 0.5 sec. EE bit ("0":PB, "1":EE) Mute when V-Mute = "H".	O
29	AFT MUTE	PWM0	"H" is putted at PCON rising and Ch position changing.	O

<table>
<tr><th>Pin No.</th><th>Name</th><th>Terminal</th><th>Description</th><th>I/O</th></tr>
<tr><td>30</td><td>VT. PULSE</td><td>PWM rmp</td><td>Waveform having experienced pulse width modulation (PWM) according to 14 bit tuning data is outputted.</td><td>O</td></tr>
<tr><td>31
32
33
34</td><td>NC</td><td>R
G
B
BLANK</td><td></td><td></td></tr>
<tr><td>35</td><td>$\overline{H_{SYNC}}$</td><td>$\overline{H_{YSNC}}$</td><td rowspan="2">Input terminal for data to specify display point of character data.
Connected to GND as not used.</td><td>I</td></tr>
<tr><td>36</td><td>$\overline{V_{SYNC}}$</td><td>$\overline{V_{SYNC}}$</td><td>I</td></tr>
<tr><td>37</td><td>$\overline{\text{SYNC DET}}$</td><td>P0B3</td><td>Terminal to input sync DET IC output and detect video signal. ''L'' when H sync is present.</td><td>I</td></tr>
<tr><td>38</td><td>B1</td><td>P0B2</td><td rowspan="2">Band switching control output terminal.
<table><tr><th>Band</th><th>VL</th><th>VH</th><th>SYPER</th><th>U</th></tr><tr><td>B0</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>B1</td><td>L</td><td>L</td><td>H</td><td>H</td></tr></table>Table 6-2.</td><td>O</td></tr>
<tr><td>39</td><td>B0</td><td>P0B1</td><td>O</td></tr>
<tr><td>40</td><td>DATA I/O</td><td>P0B0</td><td rowspan="3">Terminal for serial transfer between the automatic voltage synthesizer IC and E^2PROM.
(CS turns ''H'' only when accessing E^2PROM.)</td><td>I/O</td></tr>
<tr><td>41</td><td>CLOCK</td><td>P0A3</td><td>O</td></tr>
<tr><td>42</td><td>CS</td><td>P0A2</td><td>O</td></tr>
<tr><td>43
44</td><td>T.A CLOCK
T.A DATA</td><td>P0A1
P0A0</td><td>Used for serial communication with the timer microcomputer.
Terminal for I^2C bus control.</td><td></td></tr>
<tr><td>45
46</td><td>NC</td><td>P1C3
P1C2</td><td></td><td></td></tr>
<tr><td>47</td><td>AFT-S CURVE IN</td><td>P1C1</td><td>Terminal to input AFT voltage (tuning error voltage) from IF pack.
It detects tuning point with AFT voltage.</td><td>I</td></tr>
<tr><td>48</td><td>AT 5V</td><td>AD0</td><td>A/D converter input terminal.</td><td>I</td></tr>
</table>

6-2. IC1401 Automatic Voltage Synthesizer IC Functions

(1) Manual tuning function
- Selection between UHF, Normal and VHF can be made with pin ⑥ input voltage. Switching is made with 3-position slide switch.
- Manual tuning can be made by continuously pressing MT(+) and (−) key. Fine tuning can be made by pressing momentarily.
- Data can be stored in E^2PROM after tuning.
- AFT mute is outputted when PCON is ON and at channel switching.

(2) Auto search tuning function
- Tuning is made with sync DET IC output and AFT voltage.
- Tuning is automatically made by pressing Auto KEY.

(3) FTZ specification correspondence
- Detecting no sync, and outputting V-mute.

(4) Title OSD function

(5) DATE REC function

(6) Sound multiplex circuit control

Description of (4) ~ (6) is omitted as they are not used in this model.

6-3. Description of tuning unit operation

(1) Auto search tuning operation

a) Start

When "AT" key is pressed with CH Set SW being at VHF or UHF position, auto search tuning is started. Tuning direction is restricted to up direction only.

b) Search route and search time

(When CH Set SW is at VHF)

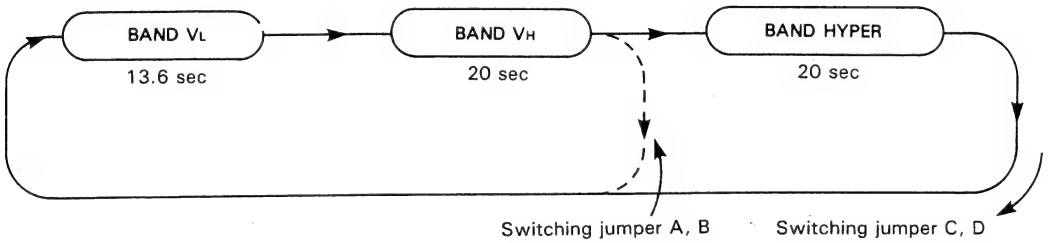
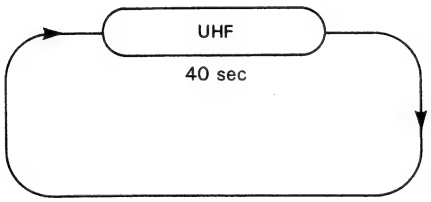


Figure 6-6.

(When CH Set is at UHF)



NOTE: Search time means the time taken when there is no station.

Figure 6-7.

c) Auto search

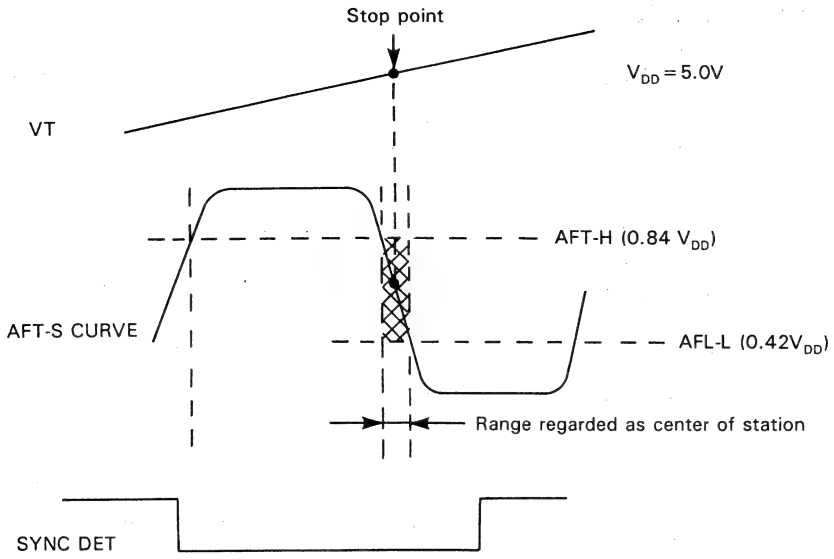


Figure 6-8. AFT-S curve at searching

Fig. 6-8 shows AFT curve and the timing of synchronizing identification signal at searching. AFT-S curve is fed into A/D input terminal pin ㊼ of IC1401. Higher section than (AFT-H), lower section than (AFT-L) and middle section in between are detected, and the range regarded as the center of station is searched.

d) Automatic detection of station

① VT (IC1401 pin ㉚) voltage is raised at fast speed until it is detected that synchronizing detecting = "L" (IC1404 pin ⑩ $\overline{\text{SYNC DET}}$) and AFT-S curve level (IC1401 pin ㊼) is higher than AFT-H (0.84 Vdd).

② VT is raised at slow speed until it is detected that AFT-S curve level (IC1401 pin ㊼) is lower than AFT-L.

③ With VT being lowered by minimal step, AFT-S curve level is detected becoming higher than AFT-L. VT data at this time is "A".

④ With VT being lowered by minimal step, AFT-S curve level is detected becoming higher than AFTL-H. VT data at this time is "B".
(If no sync is detected during search of 1 ~ 4, it is switched to fast search.)

⑤ The value of VT data (PWM) between "A" and "B" is determined through operation, and outputted. (Middle value is employed to eliminate the error caused by other signals on AFT-S curve.)

$$\text{PWM data of (A)} + \frac{\text{PWM of (B)} - \text{PWM of (A)}}{2} = \text{PWM of station center}$$

⑥ VT data and band data are stored in E^2PROM (IC1402) at stoppage, thus completing tuning operation.

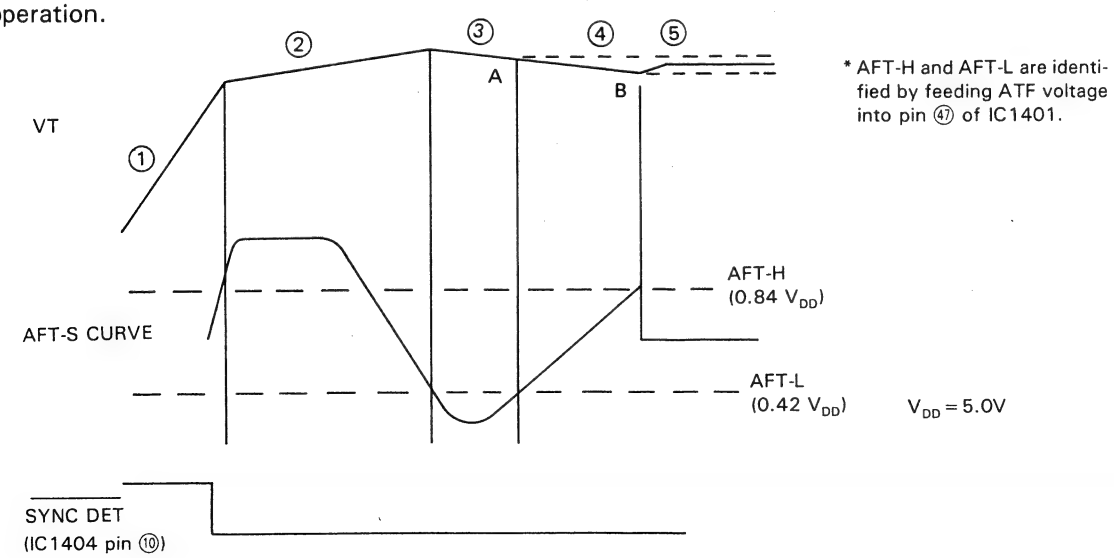


Figure 6-9.

(2) Manual tuning operation

a) Start

- When MT (+) or MT (−) is pressed in preset mode, shifting to manual search mode is performed.
- Change of constant value (△VT) is made during the first 300 msec, and in case of continuous pressing, continuous sweeping is performed.

b) Direction

Sweeping is made in the direction to raise VT with MT (+) being pressed; in the direction to lower VT with MT (−) being pressed.

c) Stoppage

- Sweeping is stopped when MT (+) or MT (−) is released, and VT data and band data at this time are written into E^2PROM. (Storing is made when KEY is released.)
- If MT (+) and MT (−) key are pressed together with other keys, VT data is not written. If other keys are released and either of MT (+) and MT (−) key remains pressed, and the other MT key is released, VT data is written.

7. Y/C CIRCUIT

7-1. DESCRIPTION OF AN3248K OPERATION (IC201: Luminance Signal Processor)

7-1-1. Main functions

(1) FM modulation/demodulation
(2) Preemphasis/Deemphasis
(3) White Clip/Dark Clip
(4) Base Band Drop Out Compensater (With CCD 1H Delay Line IC202)
(5) 1/2fH Carrier Interleave
(6) Noise Canceller
(7) Nonlinear Emphasis/Deemphasis
(8) Detail Enhancer
(9) Line Correlation Noise Canceller (With CCD 1H Delay Line IC202)
(10) Picture-Tone Control
(11) Y/C Mix
(12) FV Insert
(13) Edit

7-1-2. Description of function

(IC pin NO. whose IC REF NO. is not specified means pin NO. of IC201.)

(1) Base band drop out compensater

Base band (video signal) compensation after FM demodulation is made using CCD* (IC202) as 1H delay line. 2fsc outputted from IC501 pin ⑥ is used as CCD clock.

As transmission throughout all bands of playback luminance signal is possible with CCD, it can make more precise compensation than the system using glass delay line. While the glass delay line causes switching noise when switching FM wave, CCD causes no such noise.

While the glass delay line needs two pieces of FM demodulator, CCD needs only one demodulator.

* CCD: Charge Coupled Device

(2) REC/PB switching

Switching to REC mode is performed with EE(L) signal at pin ⑮ via D202.

(Vcc = 5.0V)

Pin ⑮ DC potential	Operation mode
0V – 1.25V	REC
2.25V – 5.0V	PB

Table 7-1.

(3) SP/LP switching

Controlled by DC potential of pin ㉓. At SP, Q204 is set to ON by SP (H) signal and pin ㉓ is made 0V, thus performing switching to SP mode. In 2-head model (except VC-A215H), pin ㉓ is directly connected to GND.

(Vcc = 5.0V)

Pin ㉓ DC potential	Operation mode
0V – 1.25V	SP
2.25V – 5.0V	LP

Table 7-2.

(4) 1/2 fH carrier interleave

In order to minimize crosstalk from the adjacent track at LP playback, carriers of CH1 and CH2 are recorded being shifted from each other by 1/2 fH (≒ 7.5 kHz) at LP recording. This conversion is performed by H.SW.P. fed into pin ㉓ via R222. At SP, pin ㉓ is made 0V and carrier interleave is not performed.

(5) FV insert

FV Insert at trick playback is controlled by FV signal fed into pin ⑪ as shown in the table below.

PB mode (Vcc = 5.0V)

Pin ⑪ DC potential	Pin ⑨ Video output
4V – 5V	Sync tip level
2V – 3V	Gray level
0V – 1V	Through

Table 7-3.

(6) Line correlation noise canceller
CCD (IC201) is used as 1H delay line. Line correlation noise canceller ON/OFF is controlled by pin ㉗ DC potential. It is set to OFF when this potential is lower than 1.25 V. Only at SP playback, Q206 is set to ON and pin ㉗ is made 0V, thus setting the line correlation noise canceller to OFF.

(7) Picture-Tone control
Controlled by DC potential applied to pin ⑬. At OPEN, it is fixed to the center, with the potential being approx. 2.5 V.

(8) Edit (used only in some models)
To prevent deterioration of picture quality at dubbing, the detail enhancer is set to OFF at recording and the function of the noise canceller is lowered and Picture-Tone control is negated (fixed to the center) at PB.
At recording, it is set to ON when pin ⑫ potential is made lower than 1.25 V. At playback, it is set to ON when pin ④ potential is made lower than 1.25 V.

7-1-3. Signal flow

(1) At recording
The video signal (1Vp-p) fed from connector CD ㉗ passes through the AGC AMP and SUB CLAMP circuits after entering via pin ⑤, being sent to pin ⑦ and the ON SCREEN MUTE circuit. The ON SCREEN MUTE circuit is controlled by DC voltage applied to pin ⑪. It exerts the function of character insertion as an ON SCREEN circuit at REC, but this function is not used in the present model, and the signal is sent through to pin ⑨ with 2.0 Vp-p. This signal level is adjusted by R203 (EE LEV ADJ) externally attached to pin ④. At PB, the ON SCREEN MUTE circuit exerts the function of FV insertion as a MUTE circuit, controlled as described in 7-1-2(5).
The signal goes out of pin ⑦ and passes through 3 MHz L.P.F. of FL201, where only luminance signal is taken out, being fed into pin ⑭. The signal fed into pin ⑭ is mixed with the signal passed through PRE AMP and H.P.F. and experiences detail enhance at the DE (Detail Enhancer) MIX section. The characteristic of detail enhancer is determined inside the IC. The signal having experienced detail enhance goes out of pin ㉑ and enters pin ㉒, experiencing sync tip clamping at the CLAMP circuit, after which it is sent to the NL (NON Linear) MIX section. It is mixed with the signal passed through the H.P.F. → LIM → FM CI section, experiening non linear emphasis, then entering the main emphasis circuit. The characteristic of non linear emphasis is determined inside the IC. At the FM CI section, signal DC voltages of CH1 and CH2 are so controlled that they are shifted from each other by approx. 2.3 mV for 1/2 fH carrier interlieve in LP mode. After entering the main emphasis circuit, the signal experiences preemphasis and undergoes white clip and dark Clip, then going out of pin ㉕ and passing through R204 to enter pin ㉖. White clip level is adjusted by R206 so that overshoot of white peak is 80 ± 4%. Dark clip level is of no adjustment and so controlled that 50 ± 10% level is achieved. The characteristic of preemphasis is determined by the values of R228, C222 and C259 externally attached to pin ㉔, and of R229 and C223 between pin ㉔ and pin ㉕.
The signal fed into pin ㉖ is subject to FM modulation and then sent to pin ㉚ with 1 Vp-p. Carrier frequency (3.8 MHz) is adjusted by R205; deviation adjusted by R204. After going out of pin ㉚, the FM signal passes through REC EQ (H.P.F.) and experiences level adjustment at R208, after which it is mixed with low frequency converted chrominance signal at Q209 and sent to the HEAD AMP via Q210 (emitter follower).

(2) At playback
The PB FM signal (4-head models: CE④, 2-head models: CE⑦) outputted from the HEAD AMP enters pin ㉘ via PB EQ. Then, after passing through D.O.C. envelop detector and double limiter, it enters the demodulator, experiencing demodulation to video signal, then entering pin ⑦ via SUB L.P.F. D.O.C detection level is determined inside the IC. D.O.C period is determined by C225 externally attached to pin ㉙.
The video signal comes from pin ⑦ passes through 3 MHz L.P.F of FL201, FM carrier component being eliminated, and enters pin ⑭, after which it passes through Pre Amp and enters the main deemphasis circuit, undergoing deemphasis, and then goes out of pin ⑰ and enters pin ⑱. The characteristic of deemphasis is determined by the constant of the component externally attached to pins ⑯ and ⑰.
The signal fed via pin ⑱ is sent to the subtracter and usually to pin ⑳ and LNC (Line Correlation Noise Canceller) MIX and NL (Non Linear) Pre Amp. The signal fed into pin ⑳ passes through IC202 CCD IH delay line, clock component being eliminated at L.P.F., and then enters pin ⑲ after experiencing level adjustment at R202. When drop out is detected, the delayed signal supplied via pin ⑲ is sent

to pin ⑳ and LNC MIX NL Pre Amp. Usually, the signal supplied via pin ⑱ and the 1H delayed signal supplied via pin ⑲ enter the subtractor, where difference component is extracted. The extracted component enters the LNC MIX section, where it is mixed with the main signal from pin ⑱, thus line correlation noise cancel being performed (in LP mode only). In case of drop out being detected, the line correlation noise canceller does not function. The signal passed through LNC MIX NL Pre Amp goes out of pin ㉑ and enters pin ㉒, then being clamped. The clamped signal enters the NC (Noise Canceller) MIX section, and at the same time a portion of the signal is fed back to LNC MIX NL Pre Amp via H.P.F → Limiter → FM CI, where it is subject to non linear deemphasis. At the NC MIX section, the signal passed through H.P.F → Limiter → L.P.F. experiences MIX and Noise Cancel. Then it goes into PB C-MIX via the APT (Aperture) CTL section, where it is mixed with playback chrominance signal, and sent to pin ⑨ via AMP → SUB CLAMP → MUTE → AMP.
The output level of pin ⑨ is adjusted to 2.0 Vp-p by R201 externally attached to pin ⑮. At the MUTE section, FV insertion at trick playback is performed.

7-2. DESCRIPTION OF TA8644N OPERATION (IC501: Chrominance Signal Processor)

7-2-1. Description of function

(IC pin NO. whose IC REF NO. is not specified means pin NO. of IC501.)

(1) REC/PB mode switching is controlled by DC potential applied to pin ⑯. PB mode is selected by applying ALPB 5V via D502. Switching to PB mode is performed with the maximum of more than 4.0 V.

(2) PAL/MESECAM switching is controlled by DC potential applied to pin ㉗ as shown in the table below.

(Vcc = 5.0V)

Pin ㉗ DC potential	Operation mode
3.3V – Vcc	NTSC *
1.5V – 2.7V	MESECAM
0V – 0.9V	PAL

* Not used

Table 7-4.

(3) SP/LP switching is controlled by DC potential applied to pin ⑰ as shown in the table below.

(Vcc = 5.0V)

Pin ⑰ DC potential	Operation mode
3.3V – Vcc	EP *
1.5V – 2.7V	LP
0V – 0.9V	SP

* Not used

Table 7-5.

(4) CH switching (CHROMA ROTATION switching) is controlled by CHROMA ROTARY signal DC potential applied to pin ⑤ as shown in the table below.

(Vcc = 5.0V)

Pin ⑤ DC potential	CH	Chroma rotation (at recording)		
		PAL	MESECAM	NTSC *
2.6V –Vcc	CH1	Shift stop	Shift stop	Advanced 90° per 1H
0V –1.6V	CH2	Delayed 90° per 1H	Shift stop	Delayed 90° per 1H

* Not used

Table 7-6.

(5) Composite synchronizing signal is fed into pin ① with positive approx. 4.7 Vp-p. Threshold values are shown in the table below.

(Vcc = 5.0V)

Input level	Threshold value
H	2.7V
L	1.7V

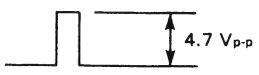


Table 7-7.

7-2-2. Signal flow

(1) At recording

The video signal (1.0 Vp-p) applied to pin ⑱ goes out of pin ⑳ after passing through the switch, after which it passes through 4.43 MHz B.P.F. (FL502), only chrominance signal band being taken out, then entering pin ㉒. The chrominance signal fed into pin ㉒ is amplified at ACC AMP so that burst signal level is constant. Then the signal enters the main converter, where it experiences low frequency conversion to 627 kHz, and enters pin ⑯ via the colour killer. The low frequency converted chrominance signal fed to pin ⑯ passes through 1.4 MHz L.P.F (FL501), undergoing level adjustment at R504, and then enters the emitter of Q209 via Q503 (emitter follower), where it is mixed with recording luminance signal.

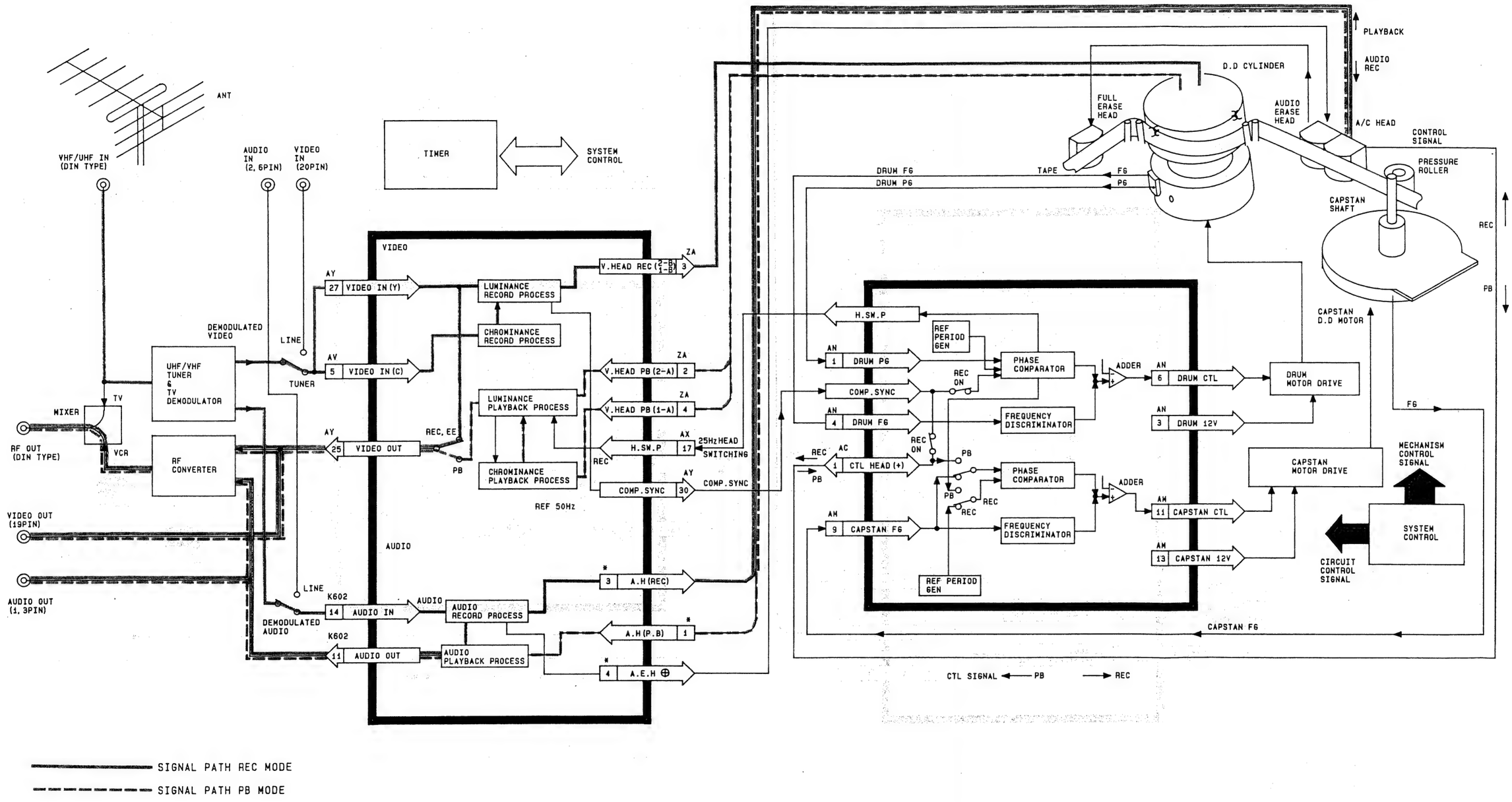
(2) At playback

The PB CHROMA signal (4-head models: Connector CE⑥, 2-head models: Connecter CE⑤) outputted from the head amp is amplified at Q507. Then it passes through L.P.F., low frequency converted chrominance signal being taken out, and then enters pin ㉔. The signal fed into pin ㉔ is amplified to a constant level at the ACC amp, sent to the main converter, where it experiences frequency conversion to 4.43 MHz, and then fed into pin ⑳. The signal fed to pin ⑳ passes through 4.43 MHz B.P.F. (FL502), being amplified at Q504, and then enters the emitter follower of Q505. In the case of 2-head models, the output of this emitter follower enters the 2H comb filter via C534. In the case of 4-head models, this output is sent to Q5551 and DL5551 (1H glass delay line) and the output of DL5551 (1H delayed signal) is supplied to the base of Q5553. Only when LP(H) signal from connector CC⑯, H.AMP.SW signal from connector CA① and FV CTL signal from connecter CA③ are all "H", that is, when the output of head amp is switched to SP HEAD side in LP trick mode, Q5555 and Q5554 simultaneously turn on and Q5553 functions, by which the 1H delayed signal outputted from DL5551 is amplified to the same level as at entering DL5551.

In this case, Q5552 turns on and Q5551 off, and the amplified 1H delayed signal is sent to the 2H comb filter of DL501. In other cases, Q5552 turns off and Q5551 on, and the signal before being 1H delayed enters DL501. This switching is performed to prevent colour disappearance caused by discontinuous phase of burst signal at Still, Slow and Double Speed Playback of LP. In 2-head models, therefore, this circuit is not used and the output of Q505 enters DL501 via C534. In 4-head models, C534 is not used. The signal fed to DL501, with luminance signal interleaved in the chrominance signal band and crosstalk from the adjacent track being eliminated, enters pin ㉘, after which it is sent to pin ㉚ via amp and the colour killer. The playback chrominance signal outputted from pin ㉚ is applied to pin ⑫ of IC201 after passing through the emitter follower of Q506, and mixed with playback luminance signal.

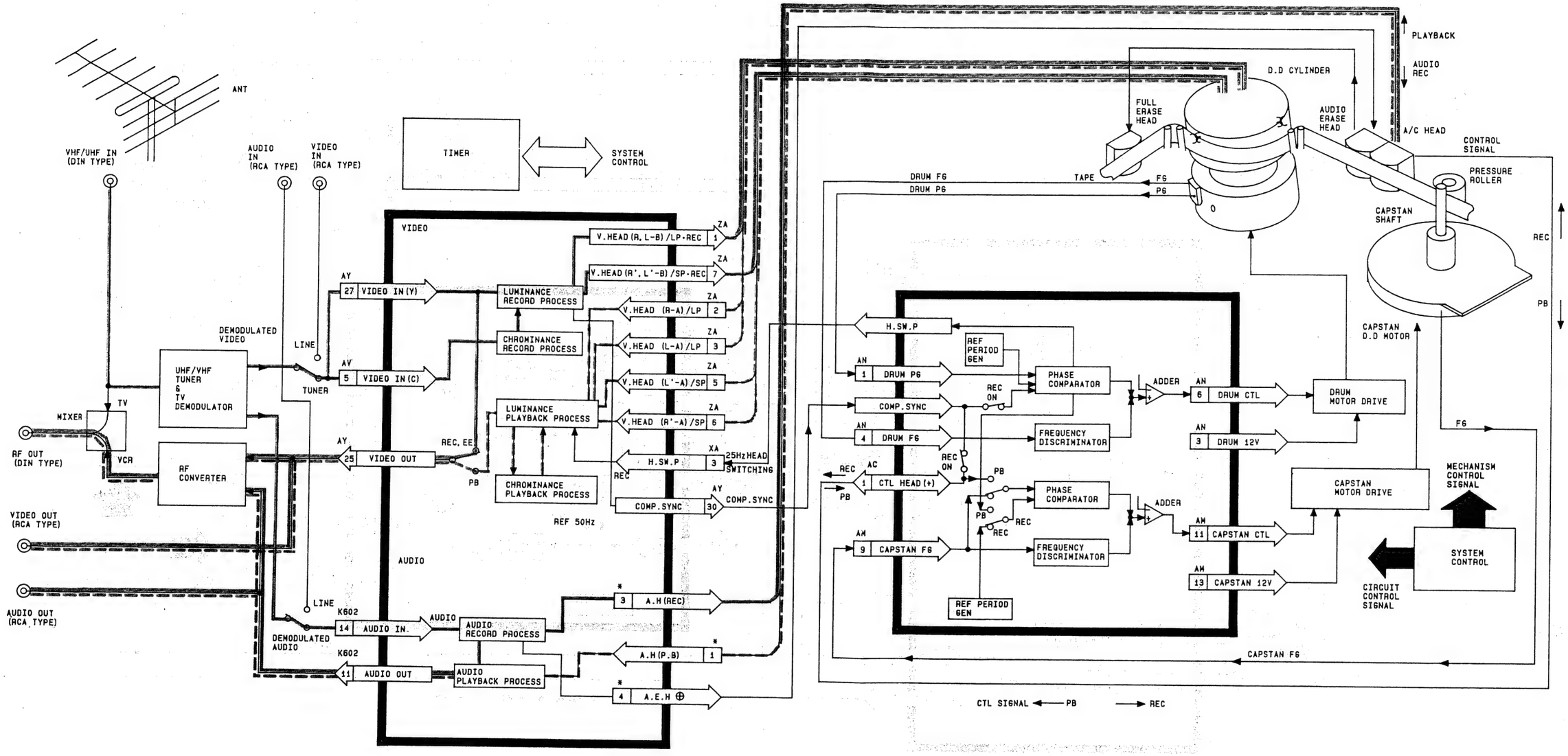
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

OVERALL BLOCK DIAGRAM (FOR 2-HEAD MODELS)



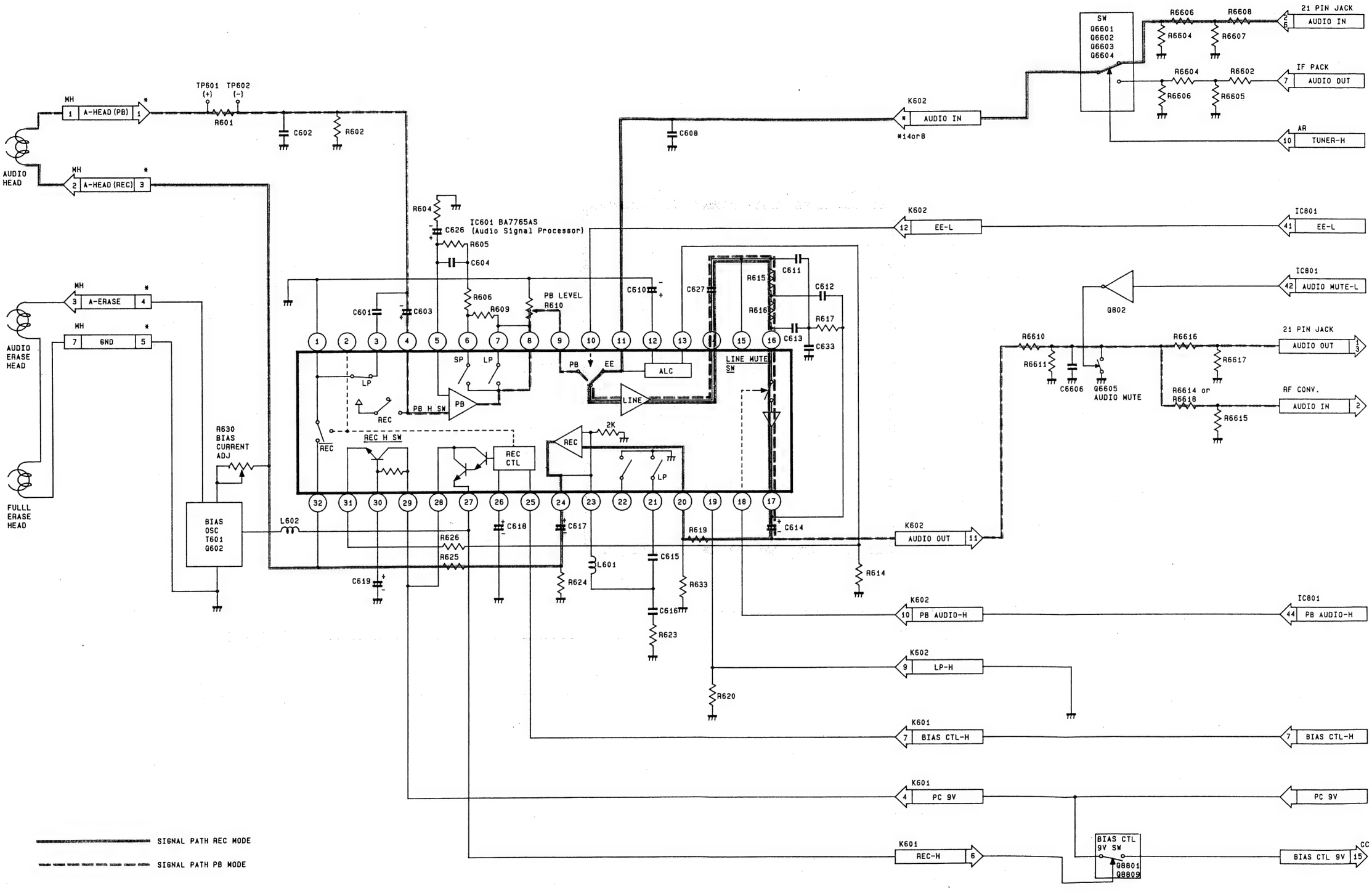
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

OVERALL BLOCK DIAGRAM (FOR 4-HEAD MODELS)



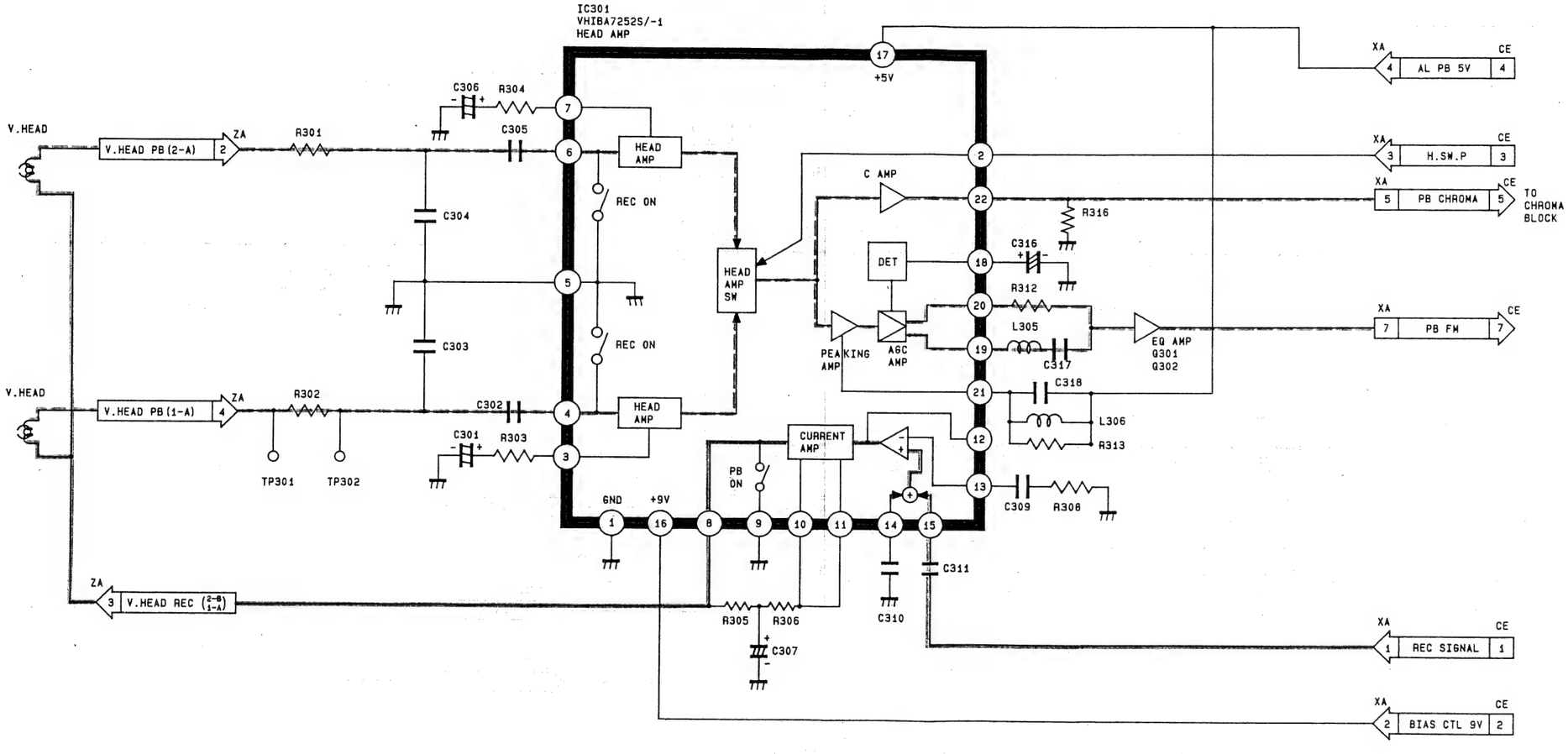
VC-A103, A116, A125,
A215, A118, A508,
A615, T620 Series

AUDIO BLOCK DIAGRAM



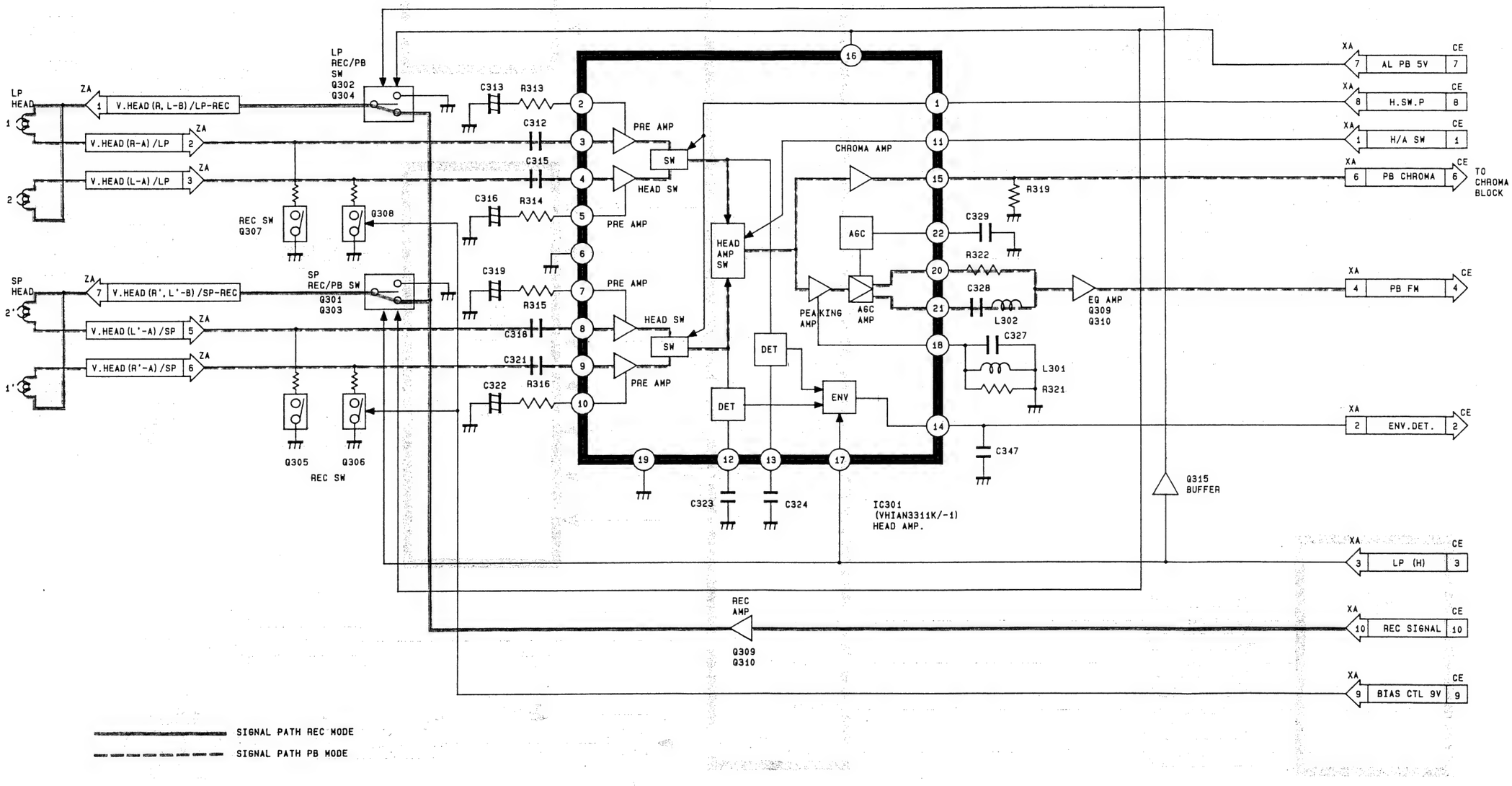
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

HEAD AMP BLOCK DIAGRAM (FOR 2-HEAD MODELS)



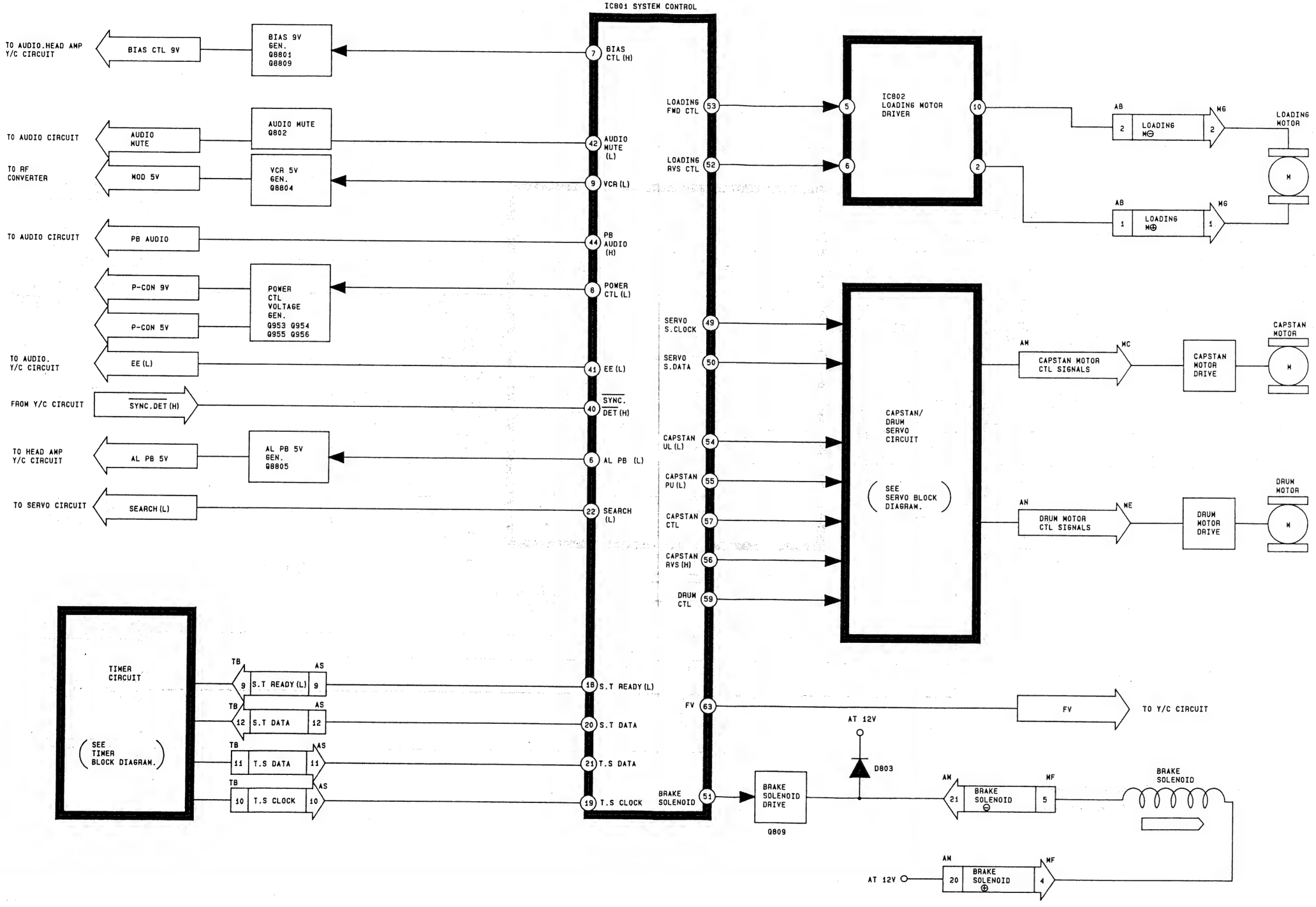
VC-A103, A116, A125,
A215, A118, A508,
A615, T620 Series

HEAD AMP BLOCK DIAGRAM (FOR 4-HEAD MODELS)



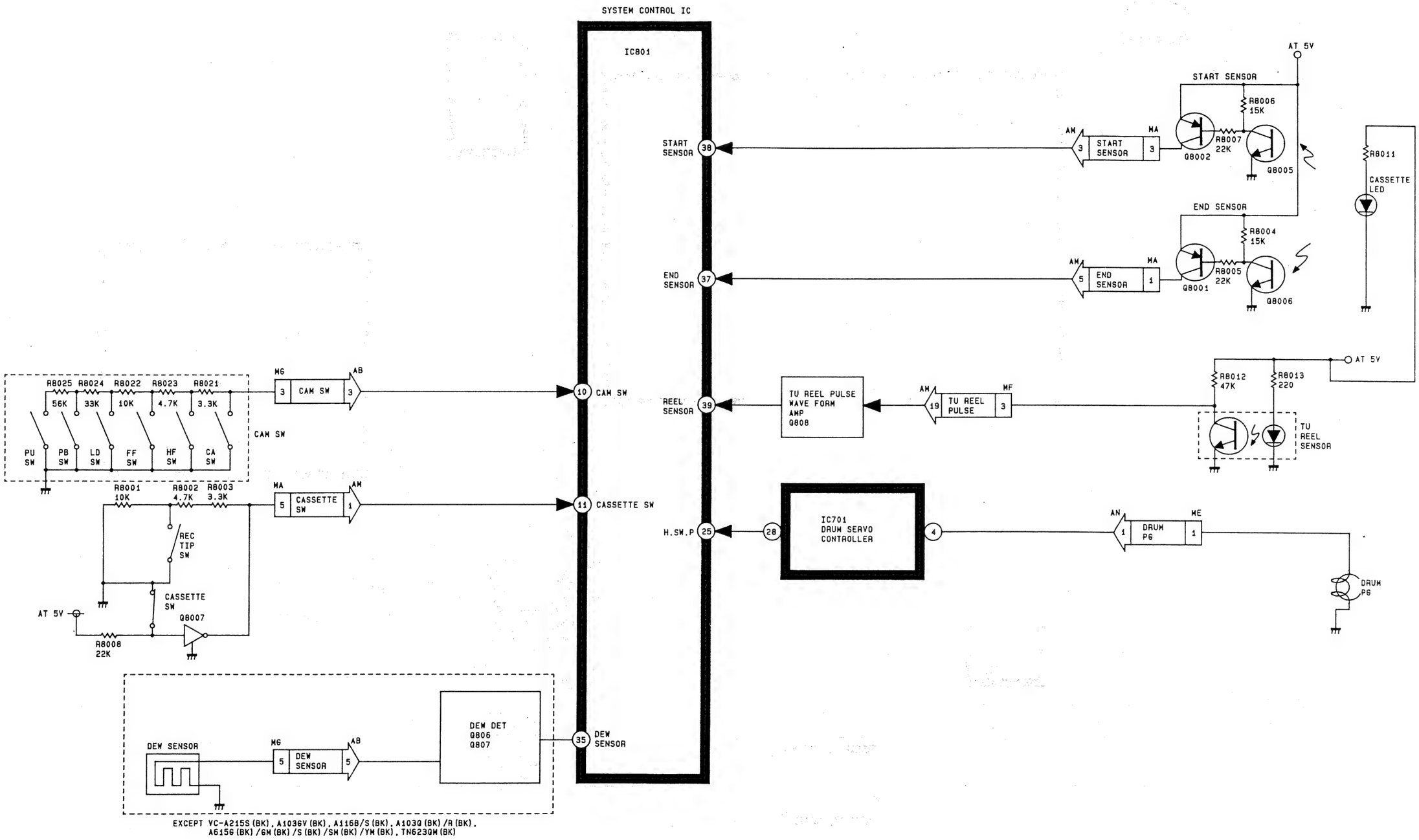
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

SYSTEM CONTROL BLOCK DIAGRAM



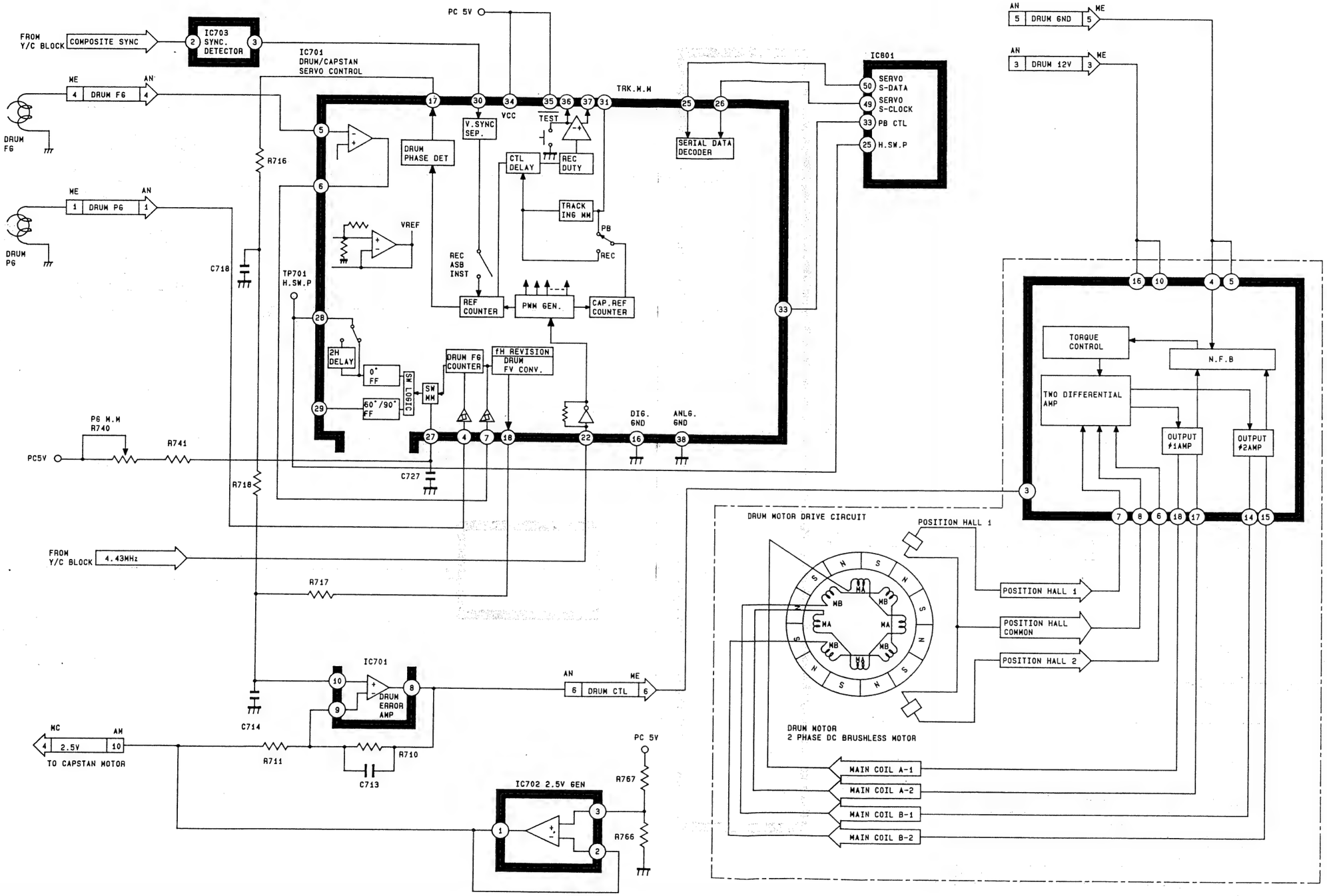
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

SAFETY DEVICE BLOCK DIAGRAM



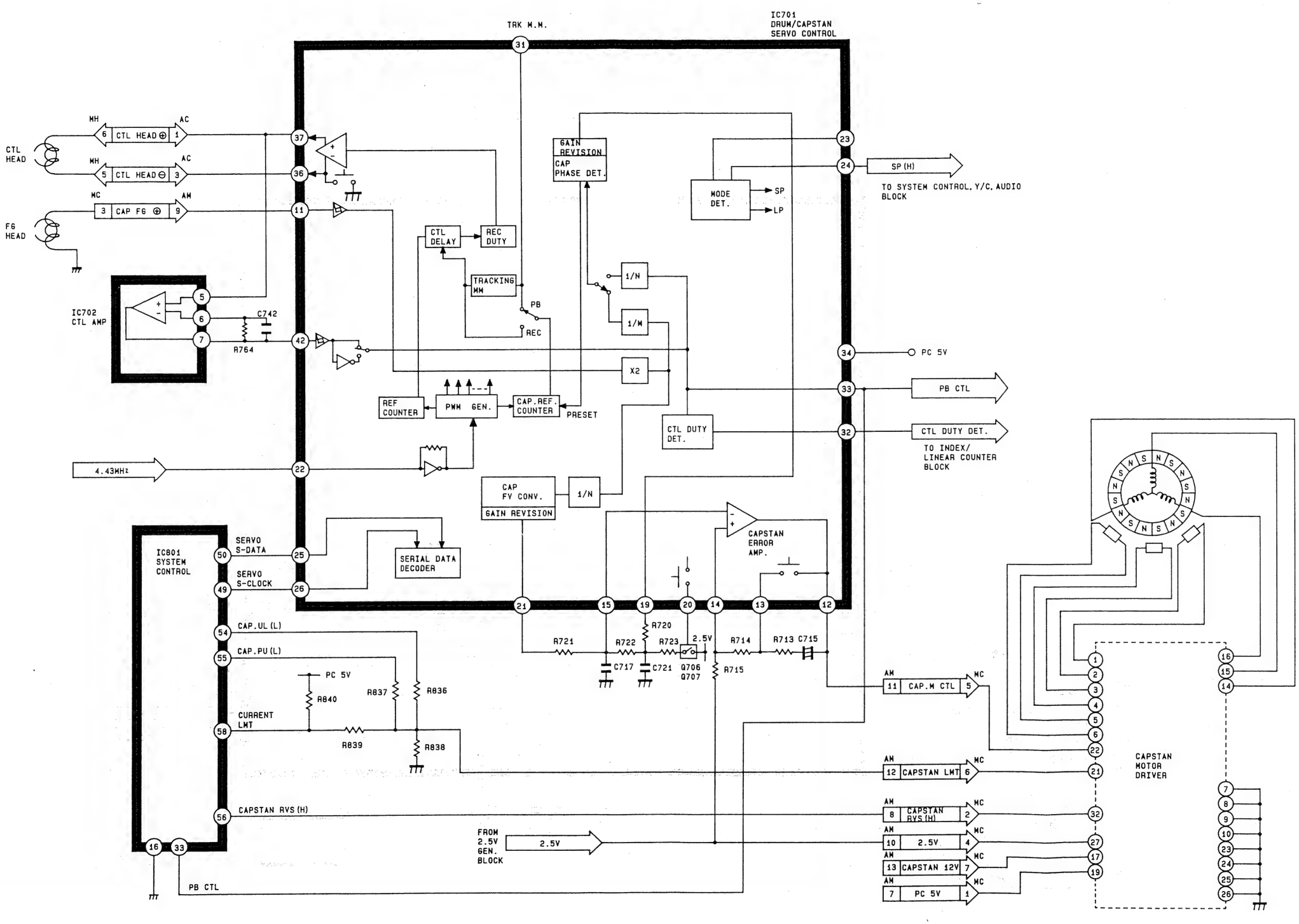
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

DRUM SERVO BLOCK DIAGRAM



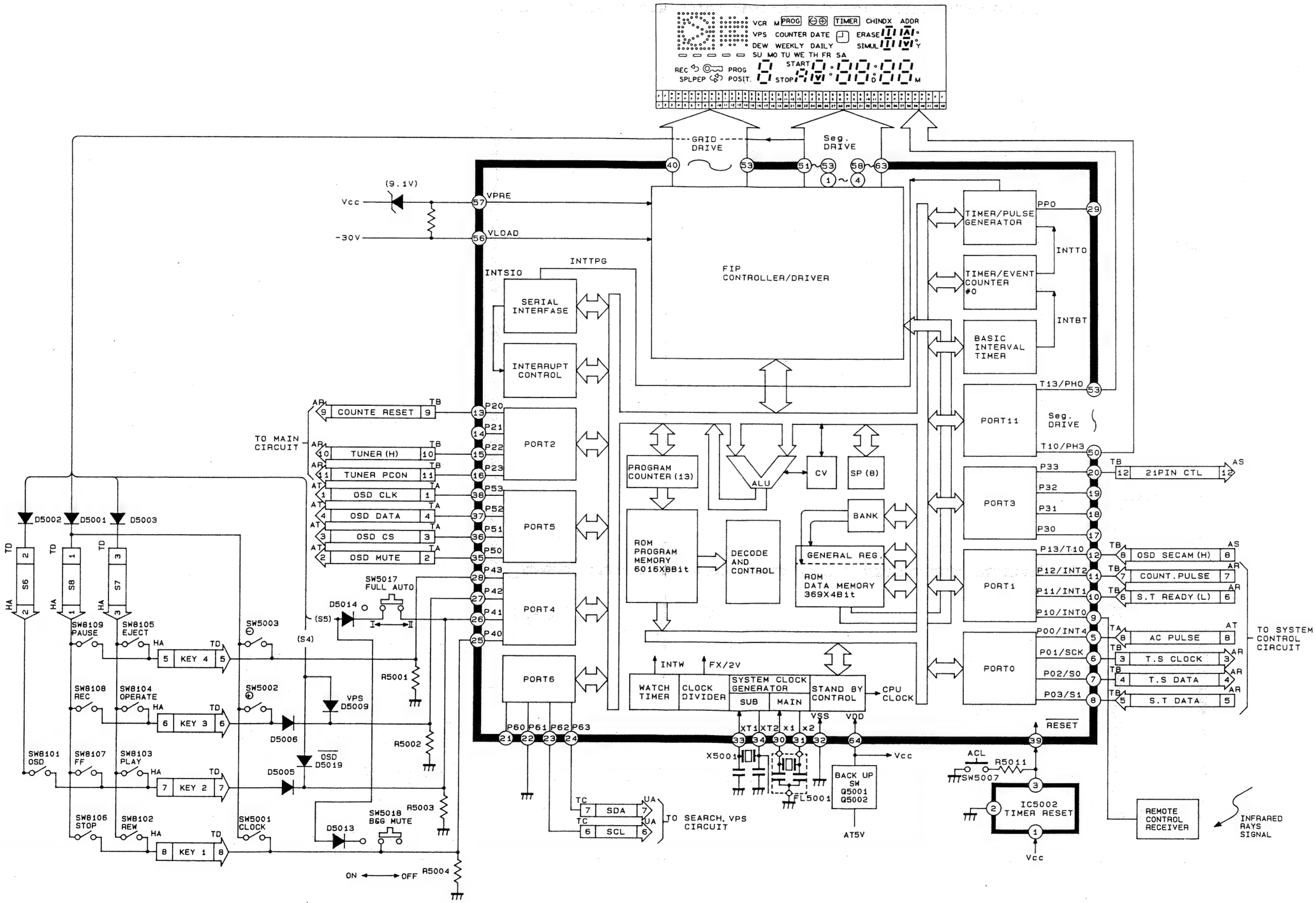
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

CAPSTAN SERVO BLOCK DIAGRAM



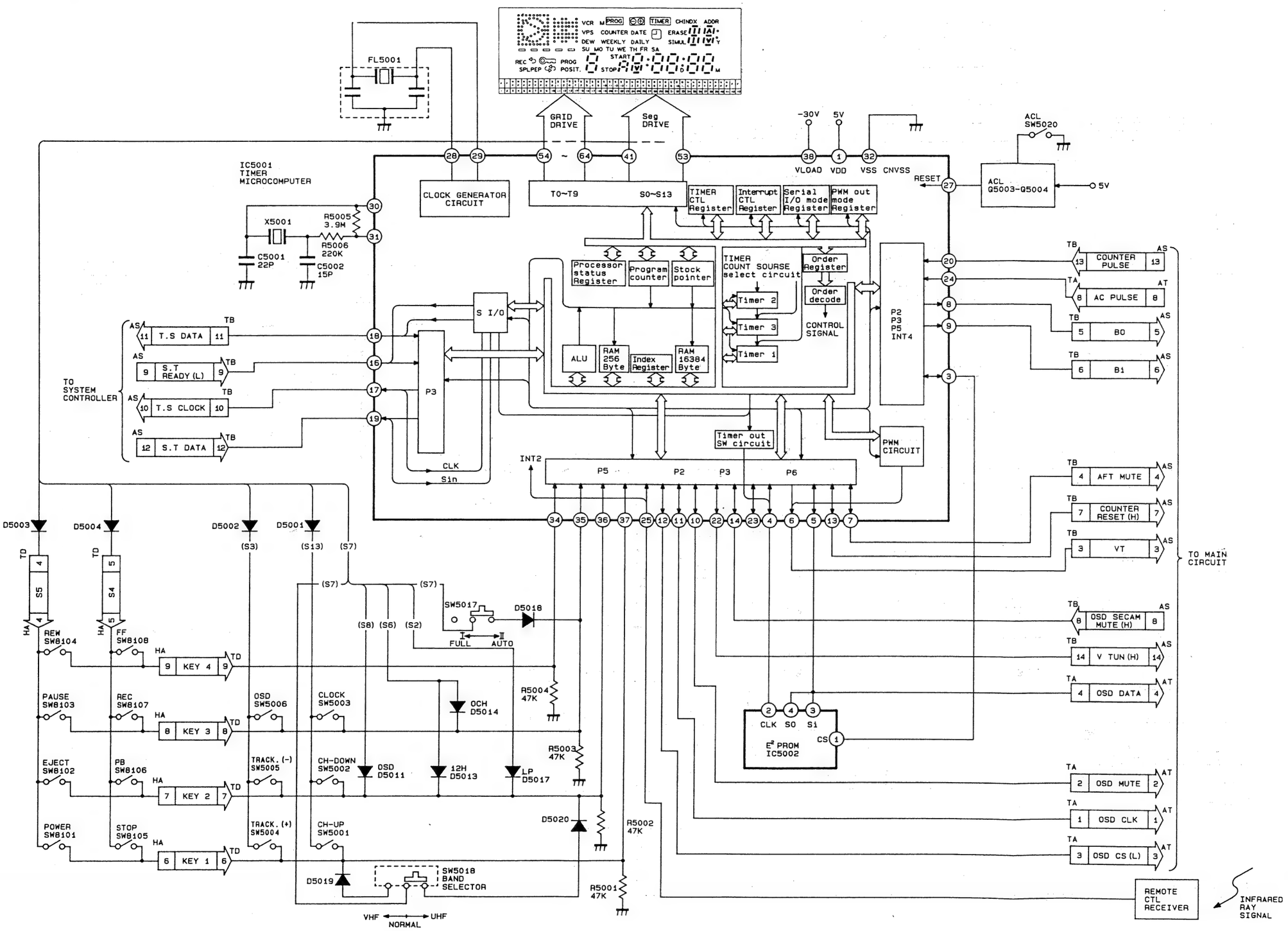
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

TIMER BLOCK DIAGRAM (VC-A103GV(BK), A215S(BK), A615G(BK)/GM(BK))



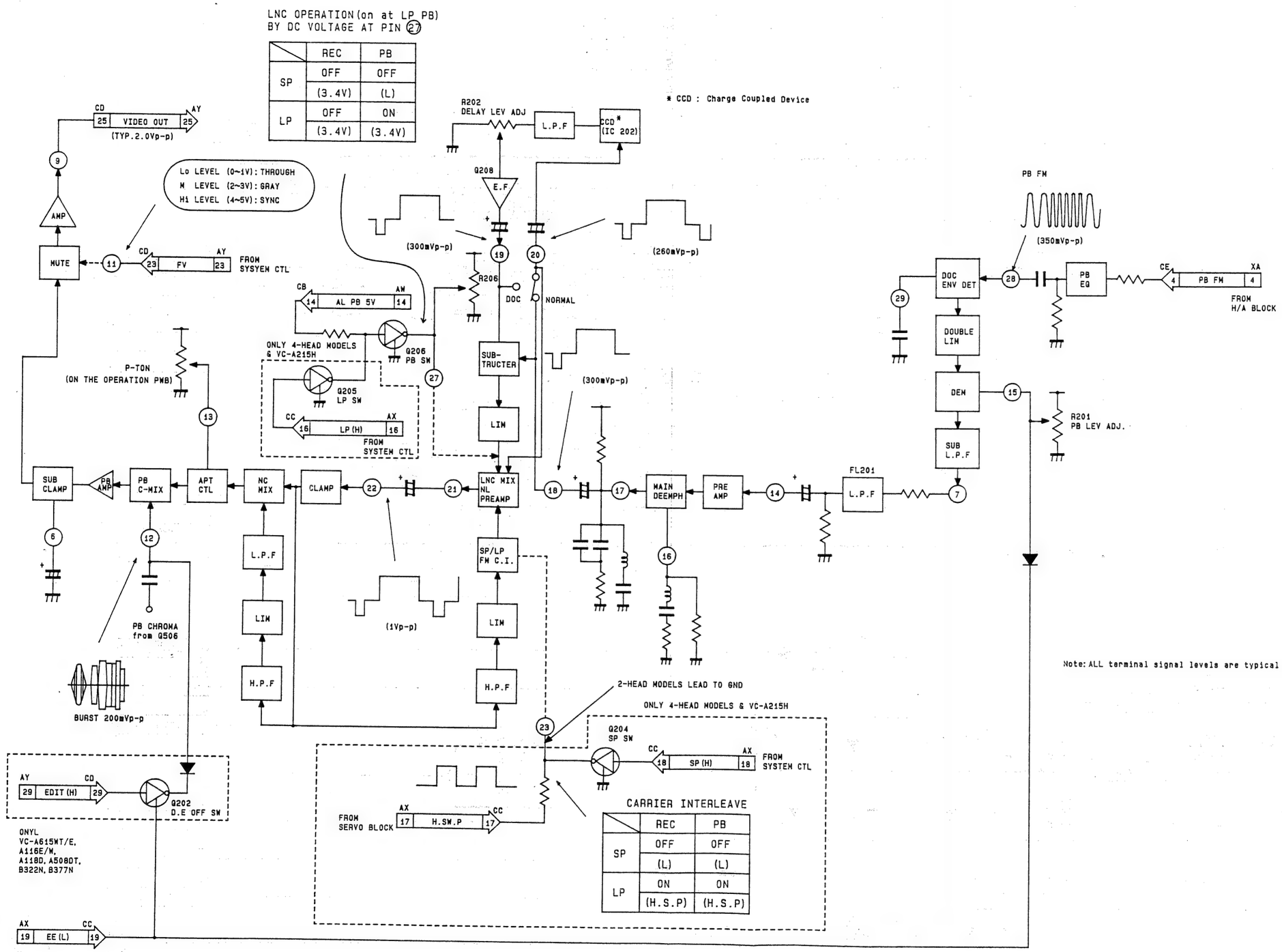
VC-A103, A116, A125,
A215, A118, A508,
A615, T620 Series

TIMER BLOCK DIAGRAM (FOR 4-HEAD MODELS)



VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

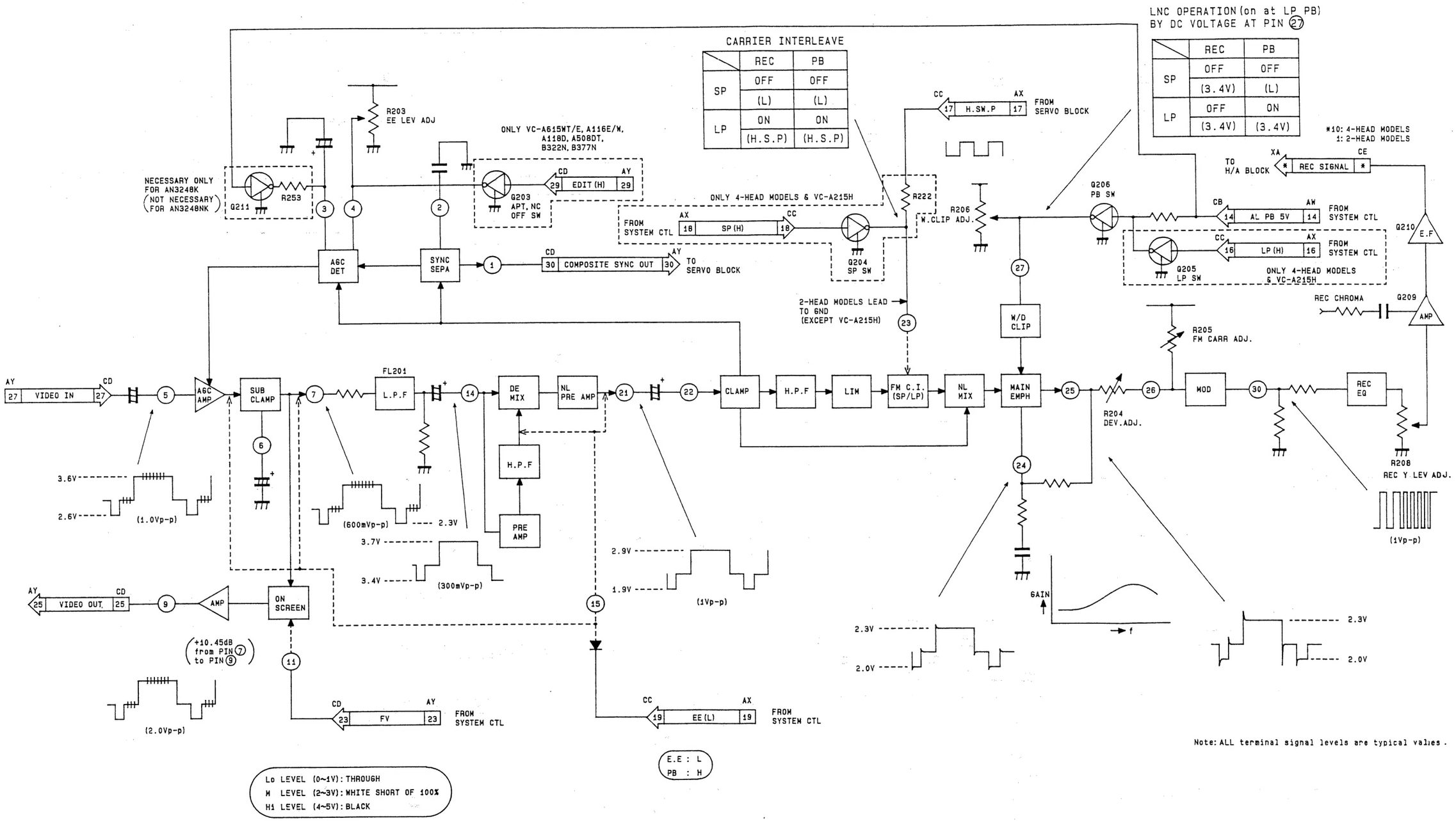
AN3248K/NK PB LUMINANCE SIGNAL LINE BLOCK DIAGRAM



Note: ALL terminal signal levels are typical values.

VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

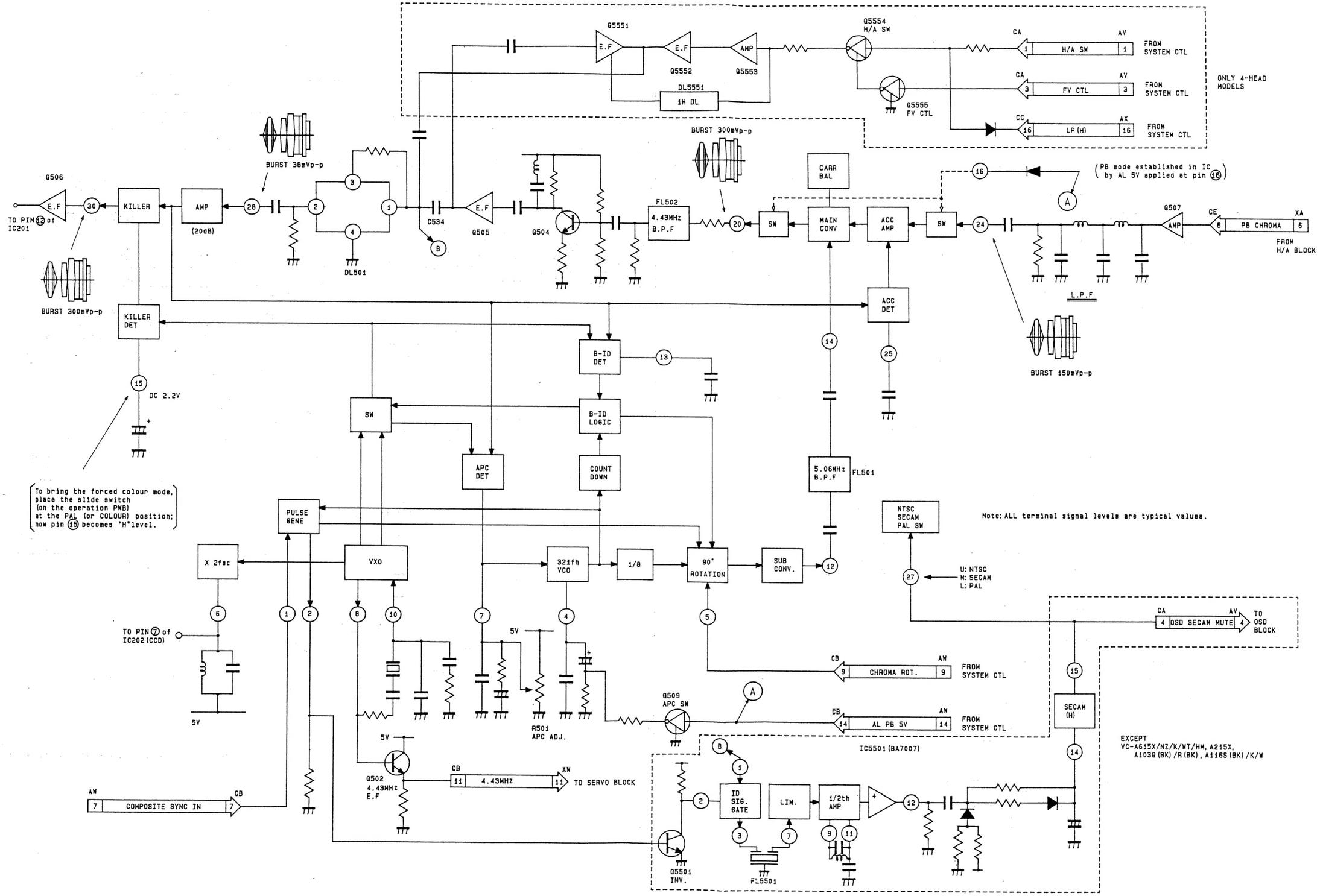
AN3248K/NK REC LUMINANCE SIGNAL LINE BLOCK DIAGRAM



Note: ALL terminal signal levels are typical values.

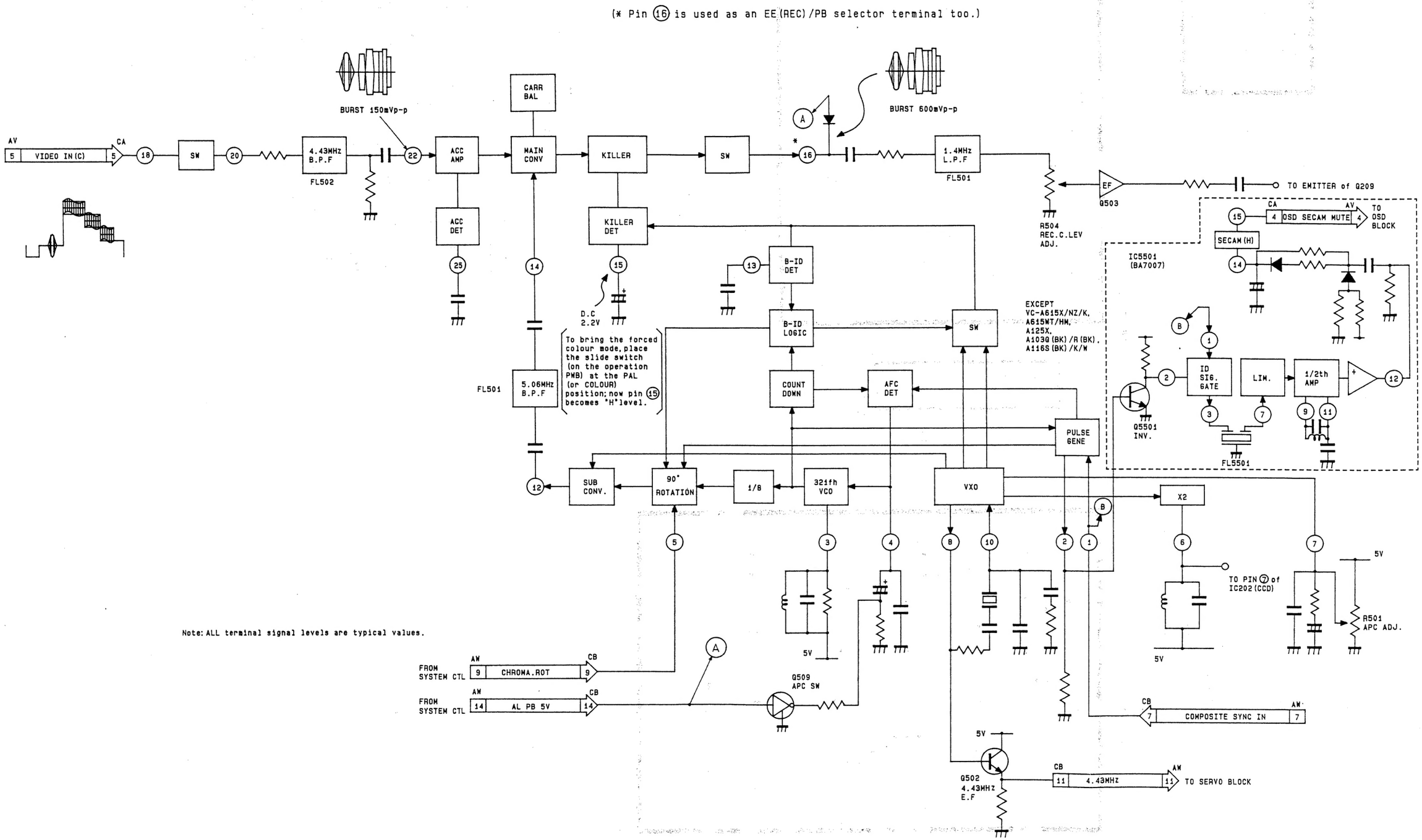
VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

TA8644N PB (PAL SYSTEM) CHROMA SIGNAL LINE BLOCK DIAGRAM

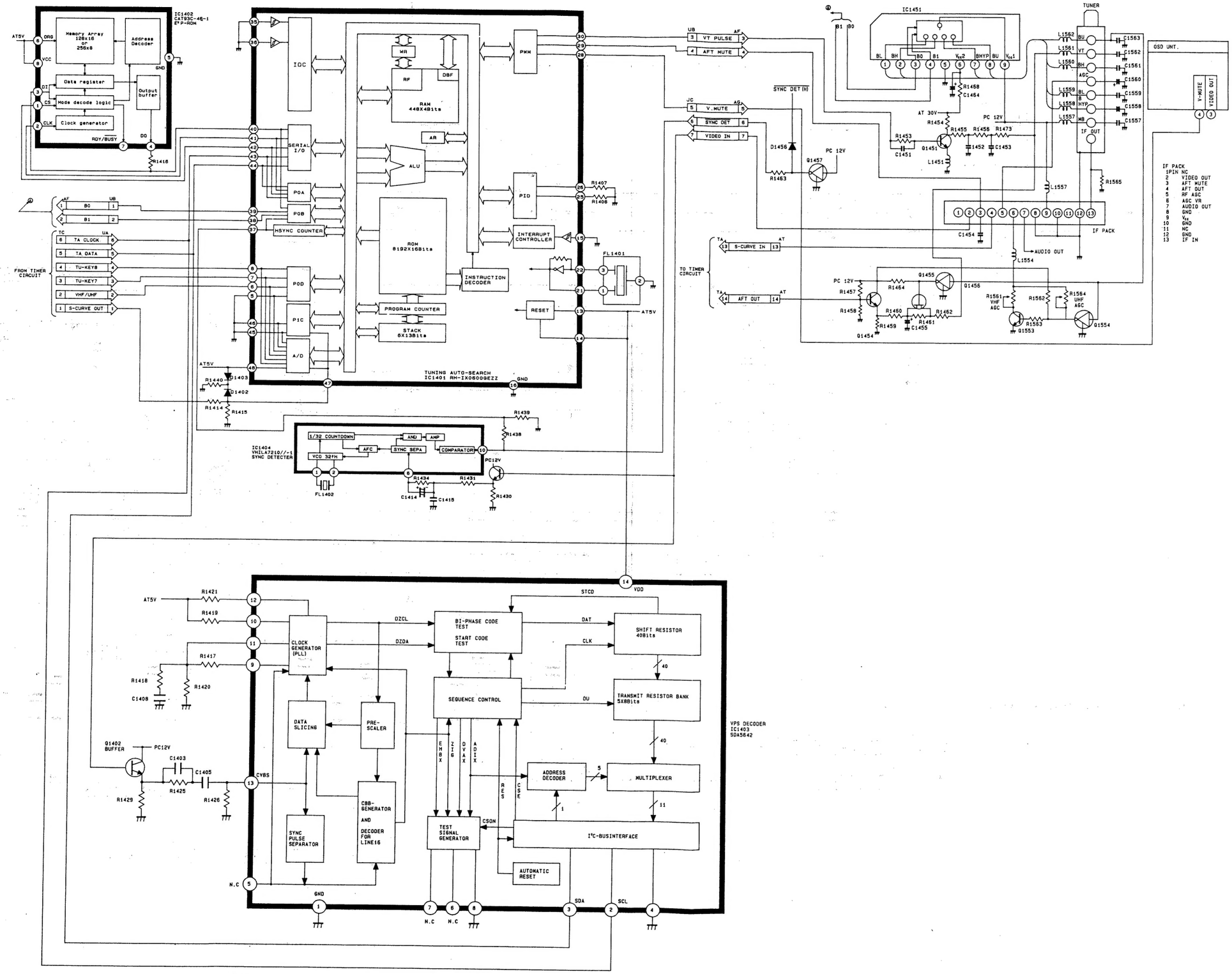


VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

TA8644N REC (PAL SYSTEM) CHROMA SIGNAL LINE BLOCK DIAGRAM



Note: ALL terminal signal levels are typical values.

VC-A103, A116, A125, A215, A118, A508, A615, T620 Series

AUTO VOLTAGE SYNTHESIZER BLOCK DIAGRAM